Hardware Design Engineer (Physical Design)

RESPONSIBILITIES

Digital Design Engineer involved in digital and circuit design of EFLX (embedded FPGA) and NMAX (inference accelerator) cores in 40nm, 28nm, 16nm, 14nm, 7nm.

- Responsible for all aspects of silicon design including:
    - PnR (RTL to GDS) and timing closure for EFLX cores in different process nodes (40nm, 28nm, 16nm, 14nm, 7nm)
    - optimization of custom digital cell library used for Look Up Tables, DSP and Interconnect switches for optimal performance, power and area (PPA)
    - timing closure (RTL to GDS) for EFLX/NMAX cores
    - Timing Verification for EFLX/NMAX cores
    - EM and IR analysis of EFLX/NMAX cores
    - DFT/ATPG pattern generation
    - Validation (testing) of the EFLX/NMAX cores

EXPERIENCE AND SKILL REQUIRED

Must have experience in at least one successfully taped out a silicon design

BSEE/MSEE with 3 or more years of relevant industry experience

Must be very smart and very motivated

Must have hands-on experience in Back-End Physical Design (RTL to GDS) PnR using tools such as Cadence Innovus or Synopsys ICC.

Preferred experience OR willing to quickly learn:

- Standard cell library development including LIB/LEF development
- Synthesis of the EFLX/NMAX cores
- Scripting language such as Perl, Python
- RTL design

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency (“green card”), or holding a current H1-B visa