Hardware CAD Design Engineer (Physical Design)

RESPONSIBILITIES

Part of the hardware design team involved in digital and circuit design of nnMAX (inference) and EFLX (embedded FPGA) cores in 40nm, 28nm, 16nm,14nm, 7nm

Primary Responsibilities:

- Installation and maintenance of foundry PDK and design kits
- Develop and support silicon design flows using industry standard EDA tools (Cadence/ Synopsys/ Mentor)
- Chip finishing (LVS/DRC) using tools such as Cadence Virtuoso, Calibre LVS/DRC flow
- Enhance and maintain projects setup and project repositories with version control software
- Maintain/enhance IT infrastructure such as Linux servers, license management
- Maintain and enhance test program used for EFLX validation chip silicon testing

EXPERIENCE AND SKILL REQUIRED

Must have experience in at least one successfully taped out a silicon design

BSEE/MSEE with 2 or more years of relevant industry experience

Must be very smart and very motivated

Must have experience in the installation of CAD tools, foundry PDK's, and design kits

Must have hands-on experience with Cadence Virtuoso

Must have hands-on experience in scripting languages such as TCL, Python, PERL, SKIL

Preferred experience OR willing to quickly learn:

- Back-End Physical Design (RTL to GDS) PnR using tools such as Cadence Innovus or Synopsys ICC.
- Timing closure tools such as Prime-Time or Tempus
- Standard cell library development including LIB/LEF development
- Synthesis of the EFLX cores

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency ("green card"), or holding a current H1-B visa