Hardware Verification Engineer

RESPONSIBILITIES

Verification Engineer involved in functional verification of NMAX Neural Inference cores and EFLX (embedded FPGA) cores in different 40nm, 28nm, 16n, 14process.

- Responsible for all aspects of verification and emulation including:
    - Setup of industry standard Verification IP flow
    - Development of verification testbench for EFLX and NMAX IP
    - Development of verification testbench for silicon validation
    - DFT/ATPG pattern generation
    - Functional verification using Verilog simulator
      Silicon Testing using bench setup to validate EFLX core

EXPERIENCE AND SKILL REQUIRED

BSEE/MSEE with at least 2 years of relevant industry experience

Must be very smart and very motivated

Must have hands-on experience in VIP development, setup of verification tools and methodology such as UVM/OVM and in developing verification plan

Must have hands-on functional coverage analysis and assertion implementation

Must have hands-on experience with standard functional simulators such as NCSIM or Questa

Preferred experience OR willing to quickly learn:

- Scripting languages such as Perl, Python, Tcl
- Understanding of RTL and ability to write RTL for EFLX cores
- Silicon validation using FPGA validation boards

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency (“green card”), or holding a current H1-B visa