InferX Inference CoProcessor SoC Design Manager or Director

RESPONSIBILITIES

Manage a silicon design team responsible for the digital and circuit design of InferX Inference CoProcessor SoCs in 7nm and beyond. (Our first InferX chip in 16nm is taping out Q4/2019)

- Responsible for all aspects of silicon design management including:
    - Backend assembly of SOC using nnMAX Inference IP and DDRx memory controller, PCIe IP and timing closure for InferX SOC in 7nm
    - Global clocks and Power gird
    - Timing Verification and closure
    - EM and IR analysis of the SOC
    - DFT/ATPG and test requirement for nnMAX core
    - Validation (testing) of the EFLX/nnMAX cores
- Technical and people management responsibility
- Work with Architecture and front-end design team as well as external Fabs, Design Services groups to support all technical interaction for a successful SoC design.

EXPERIENCE AND SKILL REQUIRED

Must have managed a team of at least 5 designers on an ASIC or SoC which included complex IP such as High Speed Serial Links, LPDDR/DDR Memory Links, CPU or GPU in a finfet process node & which is now in high volume

BSEE/MSEE with 5 years of relevant industry experience

Must be very smart and very motivated

Must be a hands-on technical leader and ability to grow the SOC design team

Proven ability to recruit, retain and manage a high-performance team

Preferred experience or ability to back teams having:

- Silicon interface with experience in Package Design
- Test requirements for complex SOC including burn-in, ATPG, At-speed, Memory BIST
- Verification of ASIC, SoC and understanding of Verification IP

Must be passionate about joining an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency (“green card”), or holding a current H1-B visa

Ability to communicate in Mandarin desirable