GF 12LP/12LP+ EFLX®4K
RAD HARD BY DESIGN

Using Rad Hard By Design standard cells and design guidelines the silicon-proven EFLX eFPGA is now available, to US Companies, in a Rad Hard by Design version.

The EFLX®4K Logic IP core is an embeddable FPGA IP core containing 2,520 Look-Up-Tables (Each LUT can be used as 6-input, or dual-5-input, with 2 independent outputs with 2 bypassable flip flops) in Reconfigurable Building Blocks (RBBs) and 21 Kbit RAM, an improved XFLX™ interconnect network, multiple clocks & scan: fully reconfigurable in-field at any time.

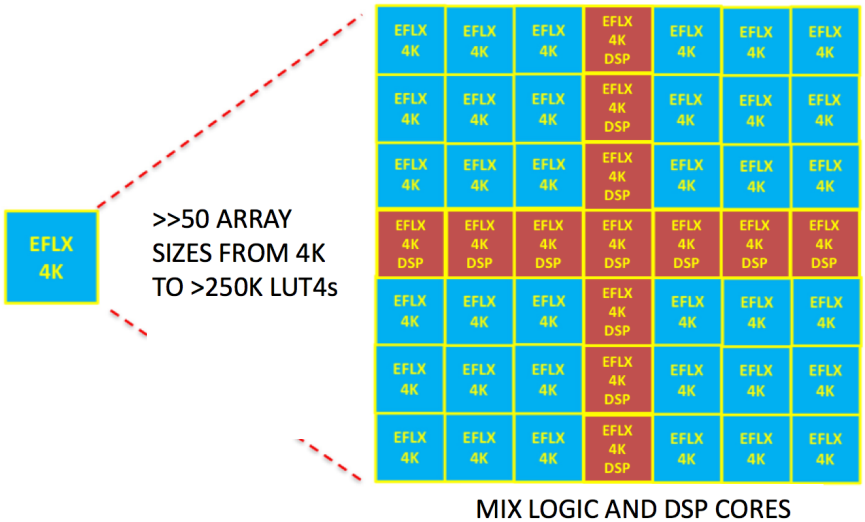
Each EFLX core is a standalone embedded FPGA. Cores can be arrayed up to at least 8x8 to create arrays >500K LUT4s. Logic and DSP cores can be mixed. And RAM can be integrated as well.

Our improved, Gen 2 XFLX™ programmable interconnect has been optimized for higher performance, especially for large arrays.

EFLX features full connectivity inside the core, and provides ArrayLinx™ interconnects at the boundary to concatenate multiple cores: array sizes are possible from 4,000 LUT4s to >500K LUT4s, with a roadmap to >1M LUT4s.

Gen 2 DFT improvements achieve 99% coverage of all faults & a new configuration load mode for test reduces test times about 100 times faster than Gen 1 to lower test costs.

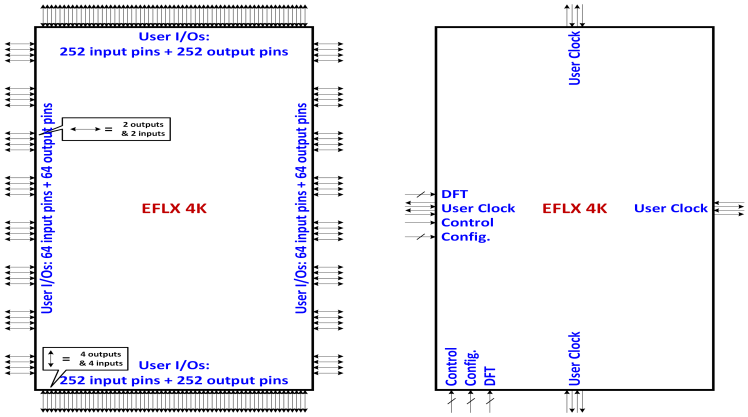
Name	EFLX®4K Core Gen 2	
Technology	GlobalFoundries 12LP/LP+	
Metal Stack	Optimized for 13 Metal Stack	
Nominal Supply Voltages (Vj)	0.6, 0.7, 0.8, 0.9	
Junction Temperature (°C)	−40 to 125	
Leakage Power	9mW (NN, 0.8Vj, 25C Tj)	
Area (mm^2)	1.57	
Clock inputs	1 to 8	
Input and Output Pins	632 input & 632 output, each with an optional flip flop	
Look-up Tables (6-input LUT with two independent outputs)	Logic/Mem Core	DSP Core *(on demand)*
	2,520 (~4.0K LUT4)	1,860 (~3.0K LUT4)
Total Flip Flops (ex DSP)	6,304	5,024
Distributed Memory (Kb)	21 Kbits	1K bits
22-bit DSP MACs	0	40
EFLX Array Sizes Possible	1×1 to >8x8	
Design-for-Test Support	Yes, 99% fault coverage	
LUT Utilization	Typically ~90%	



MIX LOGIC AND DSP CORES

flexlogix® AI + eFPGA

The EFLX 4K Core has 632 input pins and 632 output pins placed as follows: 64 West, 64 East, 252 North, and 252 South. The I/O pins provide user access to the EFLX core. Each pin has a bypassable flip flop. When multiple cores are concatenated into EFLX arrays, the pins along the abutting edges are disabled (or are used for controlling embedded RAM blocks).



GF12 EFLX4K dimensions: 0.98 wide x 1.39mm tall

Besides input/output pins, there are clock, configuration, and test/DFT pins. Each Core has an internal power grid which can be connected to the customer's digital SoC power grid. The Core also has configuration inputs on the West side and configuration inputs on the South side to load the bitstream. An AXI or JTAG interface is available for configuration. A clock mesh provides multiple connect points. The configuration bits can be read back anytime to enable checking for soft errors to improve reliability for high-reliability applications. A new test mode enables test times about 100x faster for lower test cost.

In addition to special Rad Hard by Design standard cells for storage elements, design techniques were applied to clock and reset circuits to mitigate the impact of Single Event upsets. Synopsys Premier can be used to further reduce susceptibility to Single Event Upsets by triplicating critical portions of the RTL with voting logic, if desired.

Deliverables and EDA Design Views	
Front-end Design view (with NDA)	**Back-end Design Views (with License)**
Encrypted Verilog Netlist	Encrypted Verilog Netlist with Timing Annotation & SDF
LIB	GDS-II
Footprint LEF	CDL/Spice netlist
Detailed datasheet & DSP User's Guide	Integration guidelines & assistance
Silicon validation report available	Test Vectors for DFT fault coverage of 99%
EFLX Compiler evaluation version	EFLX Compiler bitstream generation version

flexlogix AI + eFPGA ®