EFLX® Embedded FPGA
Dense, Fast, Proven, Scalable

flexlogix® eFPGA + AI

Everything You Need for an eFPGA in Your SoC

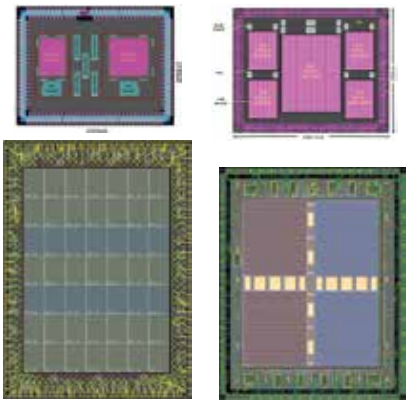
- ✔ High density & high performance similar to commercial FPGA
- ✔ eFPGA Arrays of any size by tiling proven eFPGA IP cores to the size needed
- ✔ Mix Logic and DSP tiles to suit your needs. Integrate RAM between tiles
- ✔ New nnMAX™: eFPGA optimized for AI Inference Acceleration
- ✔ Silicon proven in TSMC 12/16, 22/28, 40 & GF 12 with evaluation boards
- ✔ -40 to +125C Tj. Compatibility with your metal stack and your voltage range
- ✔ Software tools with a Graphical User Interface
- ✔ Timing files extracted from design database and available across all corners
- ✔ DFT fault coverage of 99% with special logic for 100x acceleration of test time
- ✔ Software, applications and physical design experts will support your design

First eFPGA TSMC IP Alliance Member

Flex Logix® is a TSMC IP Alliance Member based on the work it has done with TSMC over many years to develop embedded FPGA IP meeting TSMC9000 compliance for design methodology, validation in silicon & documentation. Flex Logix will continue to prove all EFLX® embedded FPGA IP in silicon with rigorous engineering checks and sign-offs.

TSMC 6/7/12/16/22/28/40, GF 12/14, Sandia 180

TSMC N7/N6	EFLX 4K	Planned for 2021
TSMC 12FFC/+/16FFC/+/FF+	EFLX 4K	*PROVEN IN SILICON*
TSMC 12FFC/+/16FFC/+/FF+	nnMAX Inference	In fabrication; available Q4/2020
TSMC 22ULP/28HPC/HPC+	EFLX 4K	*PROVEN IN SILICON*
TSMC 40ULP/LP	EFLX 1K	In design; available Q3/2020
GlobalFoundries 12LP/12LP+	EFLX 4K	*PROVEN IN SILICON*
GlobalFoundries 12LP/12LP+	EFLX 4K RADHARD	Available now
Global Foundries 12LP/12LP+	nnMAX Inference	In design; available 2021
Sandia 180	EFLX4K	*PROVEN IN SILICON*



Detailed product briefs are available for each EFLX core. Operating temperature range is -40C to +125C Tj. Multiple voltage ranges are supported. The EFLX Compiler has timing at numerous corners for each core. We can port to other process nodes in ~6-8 months when resources are available: check with Sales.

eFPGA Adoption is Taking Off!

Multiple customers have built chips using EFLX eFPGA (>10) and more are in fab and in design (>10) across multiple process nodes and multiple applications.

Customers include Dialog, Boeing, MorningCore/Datang Telecom, Sandia Labs, DARPA, Harvard, HiPer & many more that are not yet public..

Applications use eFPGA for flexibility and for acceleration in Networking, Data Center, Wireless, Mixed Signal, MCU, IoT and Aerospace.

EFLX Embedded FPGA
XFLX™, ArrayLinx™ & RAMLinx™ Interconnects

Revolutionary Interconnect Enables Density and Scalability

Traditional FPGA fabrics are only 20% programmable logic: the programmable interconnect takes 80% of the area!

Flex Logix has developed revolutionary new interconnects:
1. XFLX Interconnect: reduces the programmable interconnect area by half AND reduces the number of metal layers required. This enables density similar to commercial FPGA and compatibility with most metal stacks. XFLX utilization is typically >90%!
2. ArrayLinx Interconnect: this allows a large number of eFPGA array sizes to be built quickly using a single, silicon proven eFPGA IP core.
3. RAMLinx Interconnect: this allows any type and amount of BRAM to be quickly interleaved in an eFPGA array using silicon proven eFPGA IP cores.

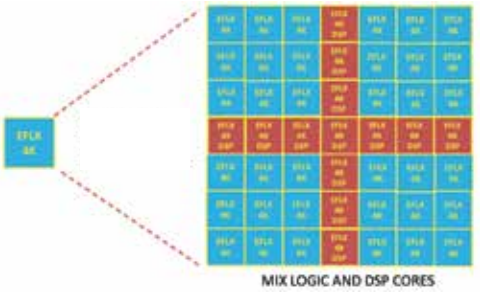
These interconnects are covered by numerous issued and pending patents in the USA and other countries.

Density & Performance Similar to Full Custom FPGA

The XFLX interconnect takes ~1/2 the area of traditional FPGA mesh interconnect, so even though we use standard cells for rapid implementation, we achieve density and performance similar to commercial FPGA. And we use only 5-7 metals layers, so we are compatible with most metal stacks.

Embedded FPGAs from 1K to 100Ks LUT4s

EFLX arrays are constructed from building blocks: the EFLX 1K core with ~1000 LUT4s and the EFLX 4K core with ~4000 LUT4s. They are eFPGAs with programmable logic, programmable interconnect, I/O, clock circuitry and configuration logic. They also have a top level ArrayLinx Interconnect which is used to build arrays of larger size by "tiling" into arrays with no GDS change. Arrays can be delivered in days & customers are encouraged to use multiple, different size arrays in a single design. All EFLX cores are proven in silicon in arrays of at least 2x2 so all array sizes are proven out. Arrays up to ~250K LUT4s are available now using EFLX4K in any mix of Logic/DSP cores. We can scale up to much larger arrays as customers require.

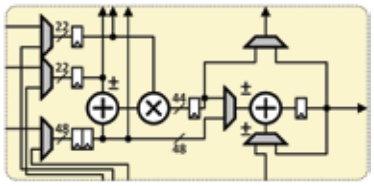


Thousands of Interface Pins

A single EFLX4K core has >1000 interface pins: 632 in and 632 out; larger arrays have much more. You can connect EFLX embedded FPGAs into wide, fast buses and wide data and control paths; the interfaces are standard CMOS so they run very fast.

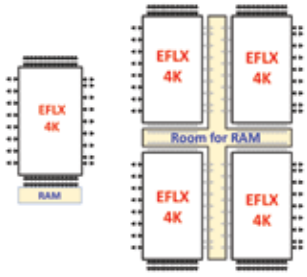
Optional MACs for DSP/AI/ML Acceleration

EFLX cores are offered in DSP versions where some of the LUTs are replaced with Multiplier-Accumulator (MAC) blocks consisting of a 22-bit pre-adder, 22-bit multiplier and 48-bit accumulator which can be pipelined for very fast DSP implementations. For AI/ML, the multiplier can be configured as two 11x11 multipliers for double the throughput.



Optional BRAM: Any Kind, Any Amount

The EFLX cores contain memory. If you require more, it can be synthesized at the edge of the array or between the cores, within the array. The EFLX Compiler software will map your RTL onto the BRAM as part of the array. We synthesize RAM from standard compilers with optional MBIST: single port or dual port, whatever size and number of blocks you want, with or without parity/ECC. We can also integrate your special memory like TCAM.



Test and Reliability Features

Test vectors are available with stuck-at fault coverage of 99% and over 80% AC coverage. Our Gen 2 Architecture has a special test mode that accelerates test speeds 100x over our first generation. For High Reliability applications we have the ability to read back the configuration bits; and "scrubbing" is also possible to re-write configuration bits periodically.

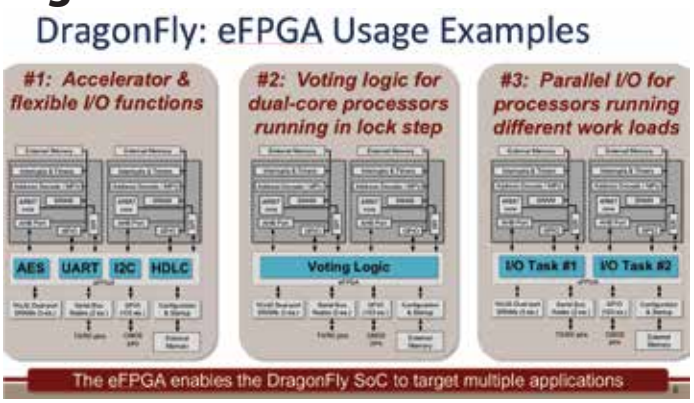
EFLX eFPGA Applications
SoC, Acceleration, AI/NN Examples

Sandia Labs First SoC with eFPGA Working in Sandia 180nm

Flex Logix developed EFLX eFPGA for Sandia for their 180nm Fab: it is Gen 2 EFLX4K.

At DAC 2018 Sandia Labs presented their implementation and architecture which they will use to build multiple SoCs and described the first SoC fabricated with eFPGA, Dragonfly.

An example of how they can reconfigure the eFPGA in their Dragonfly SoC for different use cases is shown to the right.

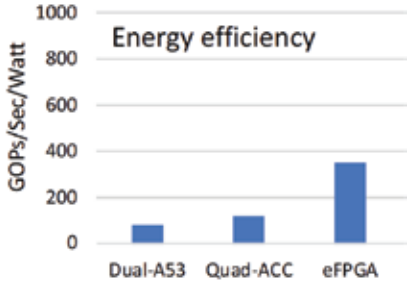


eFPGA Acceleration

An App Note on our website shows how small eFPGA arrays can accelerate heavy workloads like encryption/decryption (AES, SHA), JPEG Encoding and FFT as examples 30-100x faster than an ARM Cortex M4 processor. Since eFPGA is reconfigurable multiple workloads can be accelerated as needed.

TSMC16FFC SoC Shows eFPGA is Low Energy for AI

Harvard implemented a 2x2 EFLX array, 2 DSP and 2 Logic EFLX4K cores: ~14K LUT4s and 80 MACs. Their paper, presented at HotChips 2018, shows that of the programmable DNN Accelerators they implemented, eFPGA had similar area efficiency but much better energy efficiency.



Low Power eFPGA

EFLX eFPGA can be optimized for maximum performance OR for low power, in any given process node. Our new TSMC 40ULP design is optimized for power. Our GF 12LP/LP+ EFLX 4K comes in both a performance optimized version and a version with power management.

Rad Hard eFPGA for Space

For Space applications, we can use Rad Hard Standard Cells for storage elements and design rules for clock lines and resets to improve tolerance to Single Event upsets. Synopsys Premier can be used to triplicate critical logic for further enhancements. Sandia 180 and a version of GF 12LP/LP+ are Rad Hard.

nnMAX™ AI Inference IP

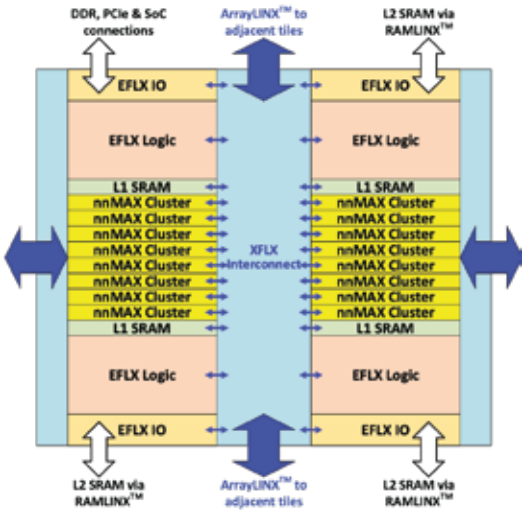
nnMAX is a high performance, modular and scalable inferencing architecture from 2 to >100 TOPS. nnMAX can run any TensorflowLite or ONNX model, or multiple models at once.

nnMAX 1K is the tile from which nnMAX arrays are constructed, same as EFLX. An nnMAX 1K tile has 1024 MACs which can process INT8x8, INT16x8 at full rate. And INT16x16 and BFloat16x16 at half rate. Activations can be mixed among INT8, INT16 and BFloat16 for maximizing precision. nnMAX 1K for TSMC16FFC is 4.5 mm^2 (6.6 mm^2 with 2MB SRAM).

nnMAX achieves very high MAC utilization, so less silicon area is needed to achieve the same throughput as other inferencing accelerators. SRAM utilization is very efficient because there is always a dedicated data path, changing layer by layer, between memory to hardware resources back to memory.

nnMAX tiles can be arrayed in any size: increasing the amount of nnMAX/SRAM results in a roughly linear increase in throughput.

nnMAX is programmed using TensorFlow Lite and ONNX Neural Networks.



EFLX Embedded FPGA
Software, Eval Boards, Business

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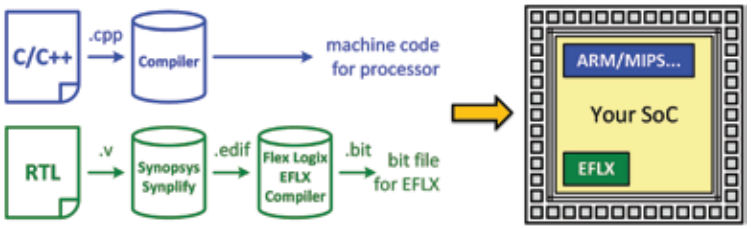
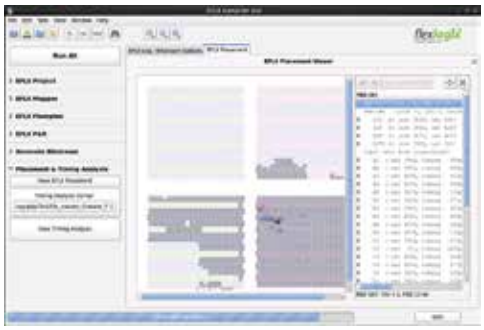
EFLX Compiler Programming

To program the EFLX array, use Synopsys® Synplify to generate an .edif file which is then input to the EFLX Compiler. You also provide an IO file which shows how the EFLX array is connected to the rest of your chip. EFLX Compiler packs, places, routes and iterates to generate optimum timing performance: if it is acceptable, EFLX Compiler generates the bitstream which when loaded into the EFLX array makes it execute your RTL.



Our GUI makes array floorplan building and timing path analysis quick and easy. New features are in development as well.



T16FFC, T28HPC+ & GF12 Evaluation Boards

Evaluation boards are available for TSMC 16FFC, TSMC 28HPC+ and GF 12LP. Bitstreams can be programmed using your Verilog to demonstrate at-speed performance and power. PVT monitors on chip so you can measure chip temperature and voltage. Interfaces to PC over USB.

Emulation Models for Cadence and Mentor

Emulation Models are available for EFLX eFPGA on both the Cadence Palladium Z1 and the Mentor Veloce Strato emulation platforms. These models have been used by us in designing our InferX X1 AI Inference accelerator and by our customers in designing their SoCs.
Emulation speeds chip development and enables architectural investigation.

About Flex Logix

- Our interconnect technology allows us to develop eFPGA that is similar to Xilinx density and speed but in much less time
- Our CEO has managed business units with up to 500 people and taken a startup from 4 people to IPO to $2 Billion Market Cap
- Our Executives all have extensive industry experience and industry recognition, including the Outstanding Paper Award at ISSCC
- Our technical team is a combination of silicon engineering, software development, architecture & system engineering
- We have dozens of issued US patents and many many more in application in multiple countries

Well Financed

We have raised ~$27 Million; our lead investors are Lux Capital and Eclipse Ventures.
eFPGA sales are growing and we are now profitable. We have a strong cash balance.
We are hiring to keep up with customer needs for eFPGA and Inference.

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www.flex-logix.com

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