System QA Engineer

Flex Logix has announced its' first AI/ML Inference Accelerator CoProcessor, InferX X1 based on our Reconfigurable Tensor Processor IP. We are gearing towards first customer ship of the InferX SoC and a family of X1 based products, and are looking for a hands-on System QA engineer to join our team to move our board products from engineering phase to production reporting to the System Engineering Director.

RESPONSIBILITIES

- Own, define and implement the X1P1 HW and System QA tasks, which include the functionality verification, 4-corner testing and error handling verification for current and future system products.
- Working closely with JDM partner, own, define and implement the HW and SW aspect of the Manufacturing Product Test Env Development for the system products. Be the lead architect on defining how to the test our product during the manufacturing process.
- Own and run the system Compatibility Test Matrix
- Be a major contributor in the customer escalation and failure analysis process. Be the first level interface to our customers regarding our system products.
- Provide review feedbacks to board architecture, schematics and layouts during the product design cycles
- Be a major contributor in the chip and board bring-up, automate and run the test scripts, and provide input to the architects on the config settings.
- Work with the System Eng Director on System QA Lab Env setup and material distribution

EXPERIENCE AND SKILL REQUIRED

BSEE/MSEE with at least 5+ years of relevant industry experience.

Must have hands-on experience for multiple generations of HW System QA cycles from early design proto-types to production. Manufacture production experience is a major plus.

Understand how to implement System level automated scripts, and has experience working with Manufacturing engineer to implement the product test environment.

On the system side, the engineer should have solid computer architecture knowledge. Understand the PCIe system architecture and the protocol. Is very familiar with DDR, I2C, USB bus protocol.

On the SW side, the engineer should be very familiar with Linux OS programming interface. Is very fluent with Python, Expect, Perl and C and C++ programming.

Past design experience with schematics, board layout and debug experiences are preferred.

The preferred engineer will be a self-learner, and is very organized, can perform the task with minimum guidance.

Must be passionate about being part of an aggressive, venture-backed startup team that is changing the way chips and boards are architecture, designed and programmed.

Must be an entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency (“green card”) or an H1-B visa