eFPGA CAD Software Design Engineer

RESPONSIBILITIES

Part of the team responsible for the netlist-to-bitstream flow for EFLX, our embedded FPGA IP, and for our new edge AI inference chip, InferX X1, including:

- FPGA Place-and-route: partitioning, placement, and routing, all timing driven
- LUT Packing: parse input netlist (EDIF, Verilog, BLIF, etc) and map netlist into EFLX logic blocks (LUTs, FFs, DSPs, RAMs, etc.), timing-driven LUT packing
- Logic Synthesis with macro recognition (RAM, Multiplier, etc.)
- Bitstream generation targeting a family of EFLX designs. FPGA size from 100 LUTs to over 100,000 LUTs
- Support existing EFLX designs and implement new algorithms for future designs to further improve QoR (quality-of-results) and runtime

EXPERIENCE AND SKILL REQUIRED

BSEE/MSEE with at least 2 years of industry experience in Software Design, likely in the EDA industry

Experience in FPGA Place and Route desirable

Must be very smart and very motivated

Preferred experience OR willing to quickly learn:

- CAD design experience of the entire FPGA back-end-flow, from synthesized netlist to LUT packing, floor-planning & partitioning, placement & routing, bitstream generation
- Knowledge and implementation experience of state-of-the-art algorithms for place & route
- Experience with algorithms mapping more than 100,000 LUT (up to 1M-LUT) FPGAs with multiple clock domains
- Multi-core programming for runtime improvement
- Windows and Linux, C++, and FPGA synthesis tools such as Synopsys Synplify

Must be passionate about being part of an aggressive, venture-backed startup team that is changing the way chips are architected, designed, and programmed

Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley

MUST have US citizenship, permanent residency (“green card”), or a current H1-B visa