EFLX eFPGA & Inference Back-end Software Development Manager (or Director)

RESPONSIBILITIES

Manage an EFLX eFPGA CAD SW development team that develops and maintains all aspects of the EFLX Compiler software tools for EFLX embedded FPGA cores and arrays which cover multiple process nodes and are highly flexible to enable arrays from 100 LUTs to over 250K LUTs with options for DSP and any kind of embedded RAM. Work closely with Silicon Engineers. The place and route tools are also used by our Inference compiler.

- Responsible for all aspects of FPGA CAD software design including:
    - Optimization of place and route tool for new Inference compiler for high speed
    - Integration with Synthesis tools such as Synopsys Synplify and soon Yosys
    - Timing-driven placement & routing for clock & data
    - Timing analyzer and debugger
    - Bitstream generator and bitstream verification
    - Graphical User Interface
    - Validation testing and regression for all releases
    - Extending high-utilization place & route tools to 500K LUTs then 1M
    - Support Yosys synthesis for our new 1K LUT EFLX eFPGA/arrays
- Technical and people responsibility
- Work with Sales and Marketing to set the software development plan, support all technical interaction with customer design and participate in customer project management meetings/teleconferences with customers. Must be willing to travel to meet with key customers.

EXPERIENCE AND SKILL REQUIRED

Must have managed a team of FPGA CAD software developers for at least 3 years.

BS/MS Computer Science, or equivalent, with 5+ years of relevant industry experience

Must be very smart and very motivated

Must be a excellent hands-on technical manager with good recruiting skills

Must have hands-on experience with C++ in a corporate CAD environment

Preferred experience OR willing to quickly learn:

- a) FPGA design experience: synthesis, placement, clock & data routing, timing analysis
- b) Develop, release, and install graphical user interface for Windows & Linux
- c) Bitstream generation and simulation, in-chip debug with FPGAs

Must be passionate about being part of an aggressive, venture-backed startup that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley and have US citizenship or permanent residency or a current H1-B visa