Inference SoC and Logic Design Engineer

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today and starts production shipments this summer.. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

Flex Logix is seeking Inference SoC and Logic Design Engineers to join our team developing the SoC RTL that controls our Inference SoCs and interfaces; and the "SoftLogic" RTL that controls the execution of the compute kernels of our neural network model operators.

RESPONSIBILITIES

Be part of our exciting team developing responsible for designing our InferX SoCs and the RTL that are used to control the execution of neural network layers (we call this SoftLogic).

The candidate must be able to work in every stage of silicon development: specification, coding, timing closure, DV and PD support, post-silicon validation, prototyping for:

- SoC design of multiple blocks communicating over Network-on-chip (NOC)

- SoC integration of NMAX engine, DDR controller, PCIe controller, and SoC management over NOC

- DMA controller for high-performance data transfer to/from host computer (through PCIe) and DDR

- SoftLogic RTL for the Reconfigurable Tensor Processor to implement neural network operators

EXPERIENCE AND SKILL REQUIRED

BS/MSEE/CE/CS with 3 years of industry experience designing commercial SoCs in production

Develop microarchitectures and identify/integrate IP to meet product requirements

Work with internal and 3rd party IP suppliers

Code/synthesize/lint RTL and complete static timing analysis

Work effectively with verification team to deliver high quality RTL

Must have hands-on experience and knowledge of SoC designs and network-on-chip designs

Must have hands-on experience designing with DMA controllers

Must be passionate about doing this job: wanting to change the world and work hard doing it

Must be entrepreneurial in spirit and an innovative problem solver

Must be willing to do what it takes to get the job done

Preferred or willing to learn:

- Knowledge of computer architecture, especially in systolic arrays
- Familiarity with memory architecture in SoC
- Experience with FPGA design and emulation
- Experience with FPGA and ASIC EDA tools
- Experience interfacing with back-end teams (silicon engineering) as well as Sales & Applications
- Experience with RTL coding in Verilog or SystemVerilog
- Experience scripting in Python or Perl
- Familiarity with C or C++ coding

MUST live in Silicon Valley or Austin TX and have a US citizenship or permanent residency (“green card”), or holding a current H1-B visa