Inference DFT Architect

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today and starts production shipments this summer.. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

RESPONSIBILITIES

DFT architect will work closely with the SOC architect, design team, embedded FPGA technologists, and logic designers to define appropriate DFT features, structures, and methodologies for our inference products. You will also work with business and operations leaders to define appropriate test coverage targets that meet quality and business needs. Finally, you will work with partners and vendors to ensure that all test goals are being achieved in production.

Our Inference Architecture is very different from other approaches combining one-dimensional tensor processors with a rapidly reconfigurable proprietary interconnect and programmable logic for control. You will need to rapidly learn this architecture, develop innovative DFT solutions and help architect follow-on SoCs for efficient and effective test.

Primary Responsibilities:

- Architect DFT solutions catered to inference products that include eFPGA
- Develop DFT flows for high-quality production
- Implement and verify DFT solutions
- Lead other team members to successfully implement and verify DFT solutions
- Interface with DFT EDA vendors
- Interface with contractors or partners
- Interface with IP providers for DFT requirements and results
- Collaborate with operations team to ensure successful and timely production of silicon
- Clearly communicate and document methods and scripts
- Clearly communicate status throughout the project

EXPERIENCE AND SKILL REQUIRED

- Extensive experience in leading DFT for high-quality products that reached high-volume production
- Proven experience in defining strategy and implementation of at least 1 high-volume production SOC
- Proven experience setting-up flows with standard EDA tools
- Deep understanding of how leading DFT industry tools work
- Deep understanding of defect density and the implication of DFT methods on physical design
- Recent hands-on experience implementing DFT on a significant SOC
- BS/MS EE/CE with 5 or more years of relevant industry experience
- Must be innovative and be able to cater solutions to particular designs
- Must have hands-on experience in scripting languages

- Must have hands-on experience in testbench creation and gate-level simulations with SDF

Preferred experience OR willing to quickly learn:

- Understanding of computer architectures for artificial intelligence
- Understanding of FPGA architectures and how to best test them
- Running logic synthesis and static timing tools

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

Must live in Silicon Valley or Austin Texas area and have US citizenship or permanent residency ("green card"), or holding a current H1-B visa