Physical Design CAD Engineer

Flex Logix is the leader in eFPGA with working silicon and customers in 40, 28/22, 16/12 and 14/12 nm nodes. We are starting now on 7/6nm EFLX eFPGA. Our eFPGA business did $16M in revenue last year and is cash-flow positive with significant growth expected in 2021.

Flex Logix also has developed an industry-leading inference architecture with superior inference throughput/$. Our InferX X1 chip and boards are sampling now and will be in production midyear.

We recently completed a $55M funding round to accelerate growth of our eFPGA and Inference businesses

RESPONSIBILITIES

Hardware CAD design engineer will work closely with design team, delivering EFLX (embedded FPGA) and nnMAX (Inference accelerator) cores in advance technology nodes. You will be responsible to enabling design team with PDK, infrastructure and flows. You will be a key contributor in increase efficiency and productivity of team.

Primary Responsibilities:

- Installation and maintenance of foundry PDKs and IPs
- Evaluate cutting edge technology nodes for various foundries
- Developing and maintaining leading edge design Infrastructure for various groups
- Maintain project repositories with industry standard version control software
- Develop and support Customer Design Environment using Cadence Virtuoso
- Develop and support Digital Design Flows using industry standard EDA tools (Cadence/ Synopsys/ Mentor)
- Collaborate with design teams and EDA vendors to adopt best practices. Develop in house design methodology to improve PPA targeting EFLX and nnMAX design.
- Enhance productivity of design team by providing automation script and innovative solution for flex-logix designs.

EXPERIENCE AND SKILL REQUIRED

- Must have experience in at least one successfully taped out a silicon design
- BSEE/MSEE with 2 or more years of relevant industry experience
- Must be very smart and very motivated
- Must have strong understanding of PDK and Standard Cell Libraries
- Must have experience in the installation of CAD tools, foundry PDK's, and design kits
- Must have hands-on experience with Cadence Virtuoso
- Must have hands-on experience with Extraction, Physical Design and Physical Verification
- Must have hands-on experience in scripting languages such as TCL, Python, PERL, SKILL
- Must have hands-on experience in version control tools such as cvs, svn, git, perforce, cliosoft SOS

Preferred experience OR willing to quickly learn:

- Place and Route using tools such as Cadence Innovus or Synopsys ICC.
- Timing closure tools such as Prime-Time or Tempus
- Synthesis using Industry standard tool such as Cadence Genus or Synopsys DC
- Standard cell library development including LIB/LEF development

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

MUST live in Silicon Valley or Austin Texas and have US citizenship or permanent residency ("green card"), or holding a current H1-B visa