SOC Physical Design Implementation Lead

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today and starts production shipments this summer. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

RESPONSIBILITIES

The Physical Design Implementation Lead will be responsible for the physical design of our future InfeX SOCs.

This position is a critical leadership position. The SOC Physical Lead will need to ensure that our InferX designs meet all PPA requirements with industry-leading quality.

Primary Responsibilities:

- Participate in the early definition of all SOCs
- Participate in selection of process technology
- Participate in the selection of physical IP
- Provide appropriate power and area estimates early in the design cycle
- Help lead internal and contract physical implementation design engineers
- Ensure that physical design methodologies and flows are state-of-the-art
- Responsible for meeting aggressive PPA targets for SOCs
- Interface with IP providers and EDA vendors
- Support planning activities
- Work closely with architects and RTL designers to ensure most-competitive product

EXPERIENCE AND SKILL REQUIRED

- Extensive experience leading SOC and IP physical implementation
- Extensive experience defining physical design methodologies
- Experience with process nodes 7 nm or smaller
- Experience with implementation of multiple-power domains via UPF
- Recent experience implementing power grids, place-and-route, clock tree, and low-power
- Recent experience defining STA environment for an SOC as well as execution
- Recent experience simulating or analyzing EM/IR
- Recent experience working with major IP providers and EDA vendors
- Excellent communication skills
- BSEE/MSEE with 10 or more years of relevant industry experience
- Must be innovative and be able to cater solutions to particular designs

Preferred experience OR willing to quickly learn:

- Understanding of computer architectures for artificial intelligence
- Understanding of FPGA architectures
- Understanding of the implications of DFT on physical design
- Methods and Use of structured-custom implementations

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

Must live in Silicon Valley or Austin area and have US citizenship or permanent residency ("green card"), or holding a current H1-B visa