Verification Director

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today and starts production shipments this summer. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

RESPONSIBILITIES

The verification director will primarily technically guide a team focused on IP and SOC verification but will also manage the verification organization.

This position is a critical leadership position for our inference and eFPGA products. This individual will be responsible for ensuring the complete functional verification of our inference and eFPGA products. Additionally, the director will be defining the critical environments and methodologies to be used. Finally, the verification director will participate in and lead many of the post-silicon validation tasks.

Primary Responsibilities:

- Manage the verification organizationr
- Responsible for functional verification and validation of inference IP and SOCs
- Ensure that methodologies used for verification are state-of-the-art
- Ensure timely completion of verification tasks
- Interface with IP providers and EDA vendors
- Drive verification planning activities
- Work closely with RTL designers and architects to ensure quick resolution of issues
- Clearly document verification plans

EXPERIENCE AND SKILL REQUIRED

- Extensive experience leading SOC and IP verification methodologies
- Extensive experience leading SOC and IP verification execution
- Experience applying automation infrastructure for verification
- Experience using formal methods
- Experience creating testbenches using UVM
- Recent experience working with major IP providers and EDA vendors in the industry
- Recent hands-on experience debugging an SOC (both in simulation and post-Si)
- Excellent communication skills
- BSEE/MSEE with 10 or more years of relevant industry experience
- Must be innovative and be able to cater solutions to particular designs

Preferred experience OR willing to quickly learn:

- Understanding of computer architectures for artificial intelligence
- Experience debugging on FPGA platforms
- Understanding of FPGA architectures
- Experience delivering SystemC or similar architecture modeling tools

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

Must live in Silicon Valley or Austin area and have US citizenship or permanent residency ("green card"), or holding a current H1-B visa