

TSMC N7/ N6 EFLX®4K *In Design*

The EFLX®4K Logic IP core is an embeddable FPGA IP core containing 2,520 Look-Up-Tables (LUTs: each is 6-input, or dual-5-input, with 2 independent outputs with 2 bypassable flip flops) in Reconfigurable Building Blocks (RBBs) and 21 Kbit RAM, an improved XFLX™ interconnect network, multiple clocks & scan: fully reconfigurable in-field at any time.

The EFLX 4K DSP core has 40 DSP MACs (22x22 multiplier with 48-bit accumulator). In the Gen2 architecture, MACs cascade up to 10 stages without using the interconnect network.

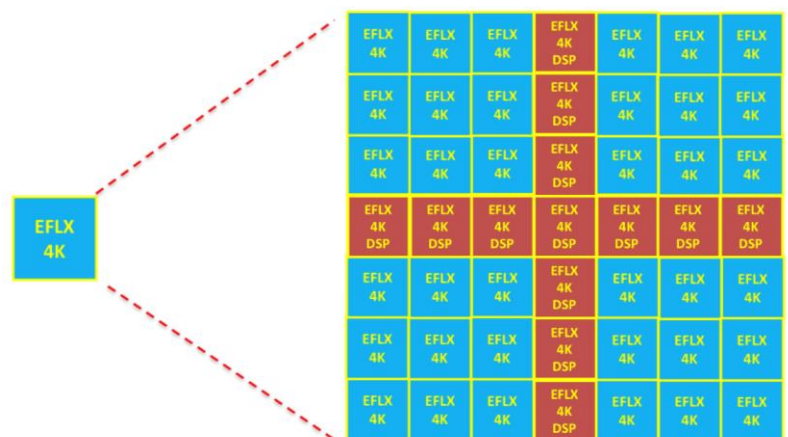
Each EFLX core is a standalone embedded FPGA. Cores can be arrayed to create arrays of >500K LUT4s. Logic and DSP cores can be mixed. And RAM can be integrated as well.

Our improved, Gen 2 XFLX™ programmable interconnect has been optimized for higher performance, especially for large arrays. Metal utilization is just 9 layers of metal and is compatible with almost all metal stacks.

Name	EFLX®4K Core Gen 2	
Technology	TSMC N7/N6	
Metal Stack	9 metal layers: 13m_1X1Xa1Ya5Y2Yy2R	
Nominal Supply Voltages (Vj)	N7: 0.675, 0.7, 0.825	
Junction Temperature (°C)	-40 to 125	
Leakage Power (mW)	6.3 (N7, TT, 0.7Vj, 25C Tj)	
Area (mm²)	0.64 (estimate)	
Clock inputs	1 to 8	
Input and Output Pins	632 input & 632 output, each with an optional flip-flop	
Look-up Tables (6-input LUT with two independent outputs)	Logic/Mem Core	DSP Core
	2,520 (~4.0K LUT4)	1,880 (~3.0K LUT4)
Total Flip Flops (ex DSP)	6,304	5,024
Distributed Memory (Kb)	21 Kbits	1 Kbits
22-bit DSP MACs	0	40
EFLX Array Sizes Possible	1x1 to > 8x8	
Design-for-Test Support	Yes, 99% coverage	
Utilization	Typically ~90%	

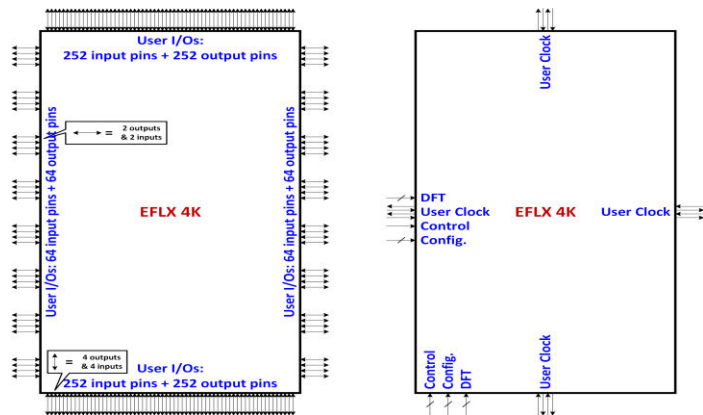
EFLX features full connectivity inside the core, and provides ArrayLinX™ interconnects at the boundary to concatenate multiple cores via the expandable network I/Os: array sizes are possible from 4,000 LUT4s to >500K LUT4s, with a roadmap to >2M LUT4s.

DFT improvements achieve 99% coverage of all faults & a new configuration load mode for test reduces test times about 100 times faster and lower test costs.



MIX LOGIC AND DSP CORES

The EFLX4K Core has 632 input pins and 632 output pins placed as follows: 64 West, 64 East, 252 North, and 252 South. The I/O pins provide user access to the EFLX core. Each I/O has a bypassable flip flop. When multiple cores are concatenated into EFLX arrays, the user I/Os along the abutting edges are disabled (or are used for controlling embedded RAM blocks).



TSMCN7 EFLX4K dimensions: ~ 0.81mm wide x 0.79mm tall

Besides input/output pins, there are clock, configuration, and test/DFT pins.

Each Core has an internal power grid which can be connected to the customer's digital SoC power grid. The Core has power control pins. The Core also has configuration inputs on the West side and configuration inputs on the South side to load the bitstream. An AXI or JTAG interface is available for configuration. A clock mesh provides multiple connect points.

Readback circuitry in Gen 2 enables configuration bits to be read back anytime to enable checking for soft errors to improve reliability for high-reliability applications. A new test mode enables test times about 100x faster to lower test costs.

Deliverables and EDA Design Views	
Front-end Design view (with NDA)	Back-end Design Views (with License)
Encrypted Verilog Netlist	Encrypted Verilog Netlist with Timing Annotation & SDF
LIB	GDS-II
Footprint LEF	CDL/Spice netlist
Detailed datasheet & DSP User's Guide	Integration guidelines & assistance
Silicon validation report available	Test Vectors for DFT fault coverage of 97+%
EFLX Compiler evaluation version	EFLX Compiler bitstream generation version

To the right is the GDS of the 16FFC+ validation chip, which includes a 7x7 array of EFLX4K cores (14 EFLX4K DSP cores and 35 EFLX4K Logic cores). The validation chip also includes numerous banks of high speed RAM, PVT monitors and a PLL for high speed testing (500MHz-1GHz) at precise Vj and Tj conditions for validation of specifications. A validation report is available from Flex Logix or on TSMC Online. An evaluation board is also available.

