EFLX® Embedded FPGA
Dense, Fast, Proven, Scalable

flexlogix® reconfigurable

Everything You Need for an eFPGA in Your SoC

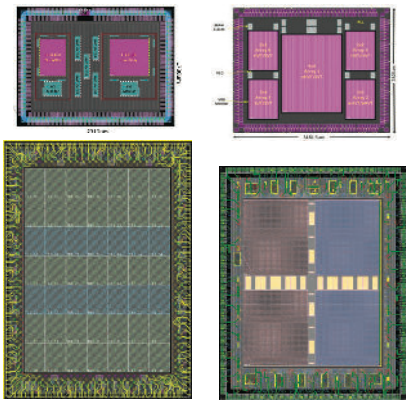
- ✔ High density & high performance similar to commercial FPGA
- ✔ eFPGA Arrays of any size by tiling proven eFPGA IP Logic, DSP or I/O tiles
- ✔ Compatible with most metal stacks. Integrate RAM between tiles
- ✔ Optimizable for super-low power or super-high performance
- ✔ Silicon proven in TSMC 12/16, 22/28, 40 & GF 12 with evaluation boards
- ✔ -40 to +125C Tj. Compatibility with your metal stack and your voltage range
- ✔ Software tools with a Graphical User Interface
- ✔ Timing files extracted from design database and available across multiple corners
- ✔ High DFT test coverage both DC and AC for high quality test
- ✔ Software, applications and physical design experts will support your design

First eFPGA TSMC IP Alliance Member

Flex Logix® is a TSMC IP Alliance Member based on the work it has done with TSMC over many years to develop embedded FPGA IP meeting TSMC9000 compliance for design methodology, validation in silicon & documentation. Flex Logix will continue to prove all EFLX® embedded FPGA IP in silicon with rigorous engineering checks and sign-offs.

TSMC 4/5/6/7/12/16/28/40, GF 12/22, Sandia 180

TSMC N5/N4	EFLX 4K	In design: PPA under NDA
TSMC N7/N6	EFLX 4K	Available
TSMC 12FFC/+/16FFC/+/FF+	EFLX 4K	PROVEN IN SILICON
TSMC 28HPC/HPC+	EFLX 4K	PROVEN IN SILICON
TSMC 40ULP/LP	EFLX 1K	PROVEN IN SILICON
GlobalFoundries 12LP/12LP+	EFLX 4K	PROVEN IN SILICON
GlobalFoundries 12LP/12LP+	EFLX 4K RHBD	PROVEN IN SILICON
GlobalFoundries 22FDX	EFLX4K	Available
Sandia 180	EFLX4K RH	PROVEN IN SILICON



Detailed product briefs are available for each EFLX core. Operating temperature range is -40C to +125C Tj. Multiple voltage ranges are supported. The EFLX Compiler has timing at numerous corners for each core. We can port to other process nodes in ~6-8 months when resources are available: check with Sales.

eFPGA Adoption is Taking Off!

Multiple customers have built >>20 chips using EFLX eFPGA which all worked first time. Dozens more are in design across multiple process nodes and multiple applications.

Customers include Renesas, Boeing, Datang Telecom, Sandia Labs, DARPA, DoD, AFRL & many more that are not yet public. ASIC companies with eFPGA experience include Socionext, GUC, Alphawave and Synapse.

Applications use eFPGA for flexibility and for acceleration in Networking, Data Center, Wireless, Mixed Signal, MCU, IoT, Automotive and Aerospace.

EFLX Embedded FPGA

Get exactly what you need in a small area at high speed

Revolutionary Interconnect Enables Density and Scalability

Traditional FPGA fabrics are only 20% programmable logic: the programmable interconnect takes 80% of the area!

Flex Logix has developed revolutionary new interconnects:
1. XFLX™ Interconnect: reduces the programmable interconnect area by half AND reduces the number of metal layers required. This enables density similar to commercial FPGA and compatibility with most metal stacks.
2. ArrayLinx™ Interconnect: this allows a large number of eFPGA array sizes to be built quickly using a single, silicon proven eFPGA IP core.
3. RAMLinx™ Interconnect: this allows any type and amount of BRAM to be quickly interleaved in an eFPGA array using silicon proven eFPGA IP cores.

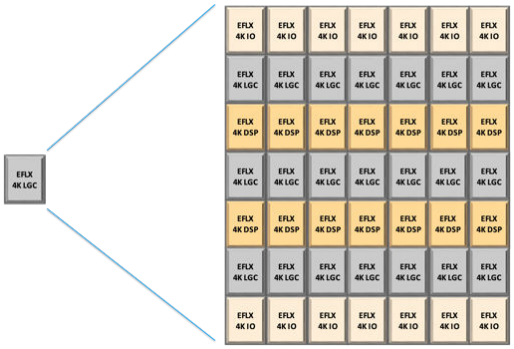
These interconnects are covered by numerous issued and pending patents in the USA and other countries.

Density & Performance Similar to Full Custom FPGA

The XFLX interconnect takes ~1/2 the area of traditional FPGA mesh interconnect, so even though we use standard cells for rapid implementation, we achieve density and performance similar to commercial FPGA. And we use only 5-7 metals layers, so we are compatible with most metal stacks.

Embedded FPGAs from 1K to Millions of LUT4s

EFLX arrays are constructed from building blocks: the EFLX 1K core with ~1000 LUT4s and the EFLX 4K core with ~4000 LUT4s. They are eFPGAs with programmable logic, programmable interconnect, I/O, clock circuitry and configuration logic. They also have a top level ArrayLinx Interconnect which is used to build arrays of larger size by "tiling" into arrays with no GDS change. Arrays can be delivered in days & customers are encouraged to use multiple, different size arrays in a single design. The largest array implemented so far is 1/4 Million LUTs. In 2023 we will offer Millions of LUTs. Large arrays can have optional "pass through" channels for SoC routing if needed.

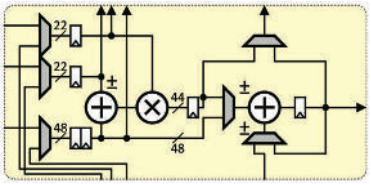


Thousands of Interface Pins

A single EFLX4K core has >1000 interface pins: 632 in and 632 out; larger arrays have much more. You can connect EFLX embedded FPGAs into wide, fast buses and wide data and control paths; the interfaces are standard CMOS so they run very fast. Our new I/O tile offers even more interface pins

Optional MACs for DSP/AI/ML Acceleration

EFLX cores are offered in DSP versions where some of the LUTs are replaced with Multiplier-Accumulator (MAC) blocks consisting of a 22-bit pre-adder, 22-bit multiplier and 48-bit accumulator which can be pipelined for very fast DSP implementations. For AI/ML, the multiplier can be configured as two 11x11 multipliers for double the throughput. MACs are pipelined 10-in-a-row; future EFLX tiles will pipeline 40.



Optional BRAM: Any Kind, Any Amount

BRAM (block SRAM) can be attached to the edge of your EFLX array using the input/output pins: you can attach any memory that you have since you control it. We integrate RAM in the array in any row between tiles: for this we have a standard, configurable RAM which can be configured as single-, two- or dual-port and configured as 32x1K, 16x2K, 8x4K or 4x8K. MBIST support is provided for array-integrated RAM. The EFLX Compiler will map RTL to RAM in the array.

Test and Reliability Features

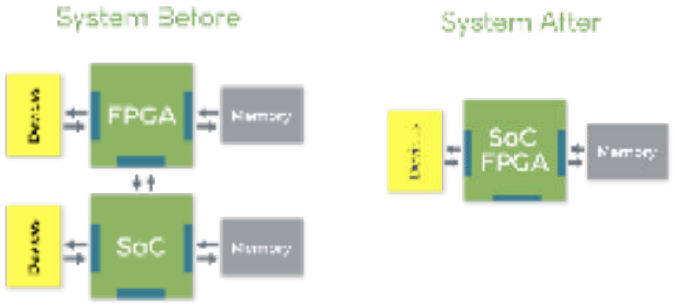
Scan test vectors are available for stuck-at (DC) and transition-delay (AC) with high test coverage. Gen 2.3 DFT is 97.8% stuck-at (DC) and 93-96% transition (AC) - we are constantly improving. Our enhanced Gen 2 architecture has special test modes that reduces test time by 5000x compared to our first generation.For arrays with integrated BRAM we provide shared memory bus interface and collateral for MBIST test. For High Reliability applications we have the ability to read back the configuration bits; and "scrubbing" is also possible to re-write configuration bits periodically.

EFLX eFPGA Applications

Make your SoC Adaptable for Changing Needs

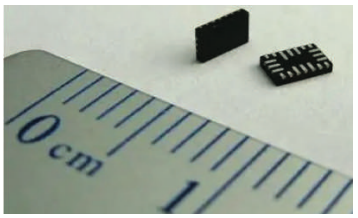
Integrate FPGA into your SoC

With eFPGA you can integrate for FPGA into your SoC while keeping the performance and the flexibility. But you cut power and cost 5-10x and double compute density. This is achievable because you get rid of the power-hungry PHYs and much of the FPGA is bussing that can be hardwared leaving the reprogrammable core. The largest eFPGA so far delivered to a customer is 240K LUTs. One of our customers is running their eFPGA at 500MHz over the full process range from -40C to +125C. Soon we will be able to deliver eFPGA of millions of LUTs.



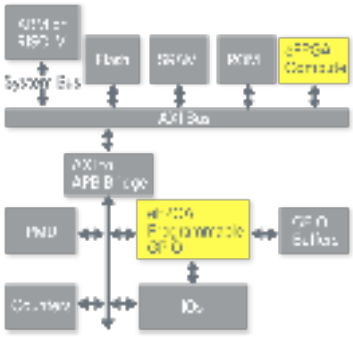
Renesas "Micro" FPGAs, super low power

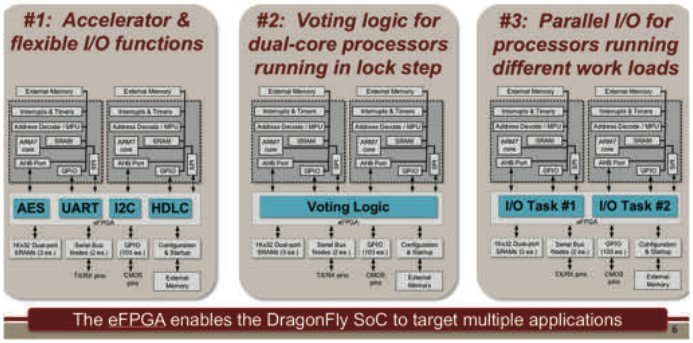
Renesas ForgeFPGAs use 40nm EFLX1K optimized for low power and power management.
They sell in volume for <50 cents, are tiny and use milliwatts. Ideal for very high volume applications.
Renesas' tool chain incorporates Flex Logix' EFLX Compiler for placement, routing, timing and bit file generation.



Fast Flexibility for MCUs+SoCs like Sandia Labs

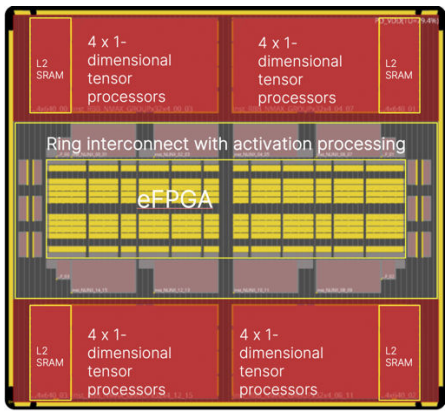
4-8K LUTs of eFPGA on the IO bus can enable you or your customer to define any GPIO: any flavor of UART, any flavor of SPI, etc. No need to do a mask spin for an odd IO requirement or to force the customer to use an FPGA to interface. eFPGA on the compute bus gives a programmable co-processor that implements workloads like compression and encryption that use FPGA's parallelism to run much faster than the host MPU. Sandia Labs uses EFLX for flexible IO and accelerators both on their Dragonfly SoC, as they showed in their DAC presentation (below right).





eFPGA for Fast, Flexible Control Path

Integrating FPGA into your SoC can cut power and cost 5-10x while maintaining full speed and flexibility. But some customers want to do even better and some customers have SoCs in planar process nodes. In working with customers, and working on our own AI architecture (shown to the right), what we realized is that in many cases the best power/performance/area comes from hardening the data path in the FPGA (in our AI compute we have 16 1-dimensional tensor processors that each have 64 MACs and a 2D weight matrix: the area they take is far less than using FPGA MACs. But we connect the 16 tensor processors using a programmable interconnect so we can configure them for different types of operations). With the data path hardened we then use eFPGA as the control path: a very high performance state machine that controls the configuration and the execution of the data path - we run at 533MHz worst case in 16nm and 800Mhz in 7nm. We can work with you on applying this concept to your needs.



Rad Hard eFPGA for Space

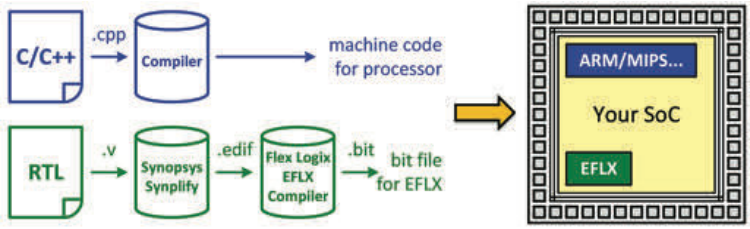
For Space applications, we can use Rad Hard Standard Cells for storage elements and design rules for clock lines and resets to improve tolerance to Single Event upsets. Synopsys Premier can be used to triplicate critical logic for further enhancements. Sandia 180 and a version of GF 12LP/LP+ are Rad Hard.

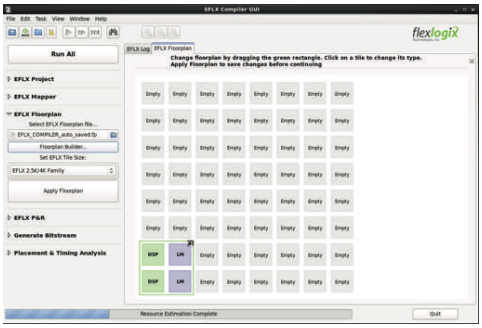
EFLX Embedded FPGA
All the tools you need

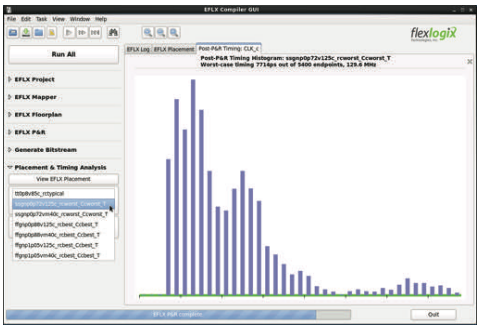
flexlogix reconfigurable

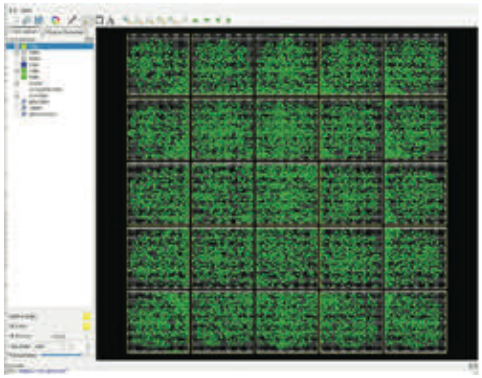
EFLX Compiler Software

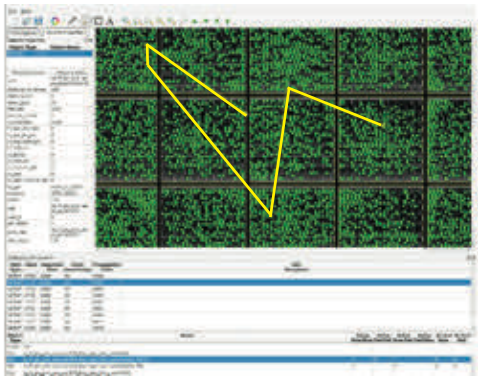
The EFLX Compiler has been in use by dozens of customers for years. It is centered on a common database. It is driven using industry standard Tcl scripting APIs or an advanced GUI interface. Input is EDIF or Verilog generated by Synopsys Synplify or other synthesis tools. Timing constraints are specified using industry standard Synopsys Design Constraints (SDC). Timing can be analyzed at any step in the place and route flow to help optimize critical paths for high perfomrance designs. Once timing is acceptable the EFLX compiler generates a bistream for loading into the EFLX array for execution.









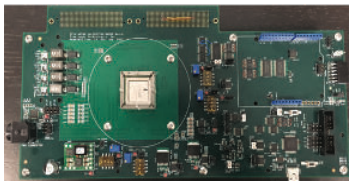


Above and to the left are some screen shots from the EFLX Compiler GUI. Above left shows the screen for selecting the array size in number of rows and columns; and which tile are Logic, DSP or IO. In the middle is a 5x5 array that has been placed. Above right is a timing browser for examing/debugging critical paths. And to the left is a timing histogram of all the critical paths in an array. These are just some of the GUI tools available for the designer.

Our EFLX Compiler is available for evaluation so you can run your RTL on any of our process nodes to verify performance and evaluate the compiler's ease of use and capabilities.

T16FFC, T28HPC+ & GF12 Evaluation Boards

Evaluation boards are available for TSMC 16FFC, TSMC 28HPC+ and GF 12LP. Bitstreams can be programmed using your Verilog to demonstrate at-speed performance and power. PVT monitors on chip so you can measure chip temperature and voltage. Interfaces to PC over USB.



About Flex Logix

- Our interconnect technology allows us to develop eFPGA that is similar to Xilinx density and speed but in much less time
- Our CEO has managed business units with up to 500 people and taken a startup from 4 people to IPO to $2 Billion Market Cap
- Our Executives have extensive industry experience and industry recognition, including the Outstanding Paper Award at ISSCC
- Our technical team is a combination of silicon engineering, software development, architecture & system engineering
- We have >60 issued US patents and patent applications; as well we have patents in Europe and China

Well Financed

We have raised >$90 Million; our lead investors are Lux Capital, Eclipse Ventures and Mithril Capital. eFPGA sales exceed $30 Million and are growing. We have a strong cash balance.

LUX ECLIPSE MITHRIL

www.flex-logix.com

01/2023TG