EFLX eFPGA

February 2023 FLEX LOGIX
Flex Logix Improves Reconfigurable Computing By 5-10x (in the same process node)

~60 US Patents and Applications

- FPGA interconnect with 1/2 transistors and 1/2 metal layers
- Self-connecting compute tiles arrayable for scalable capacity and compute
- Rapidly reconfigurable, eFPGA-controlled tensor processors

Embedded FPGA: Xilinx performance and density at 5-10x lower cost and power
Flex Is #1 in eFPGA - EFLX Adoption is Accelerating

Mature eFPGA products
• 23 chips working Si
• 9 chips in development
• Japan, China, USA, Europe
• Multiple foundries & nodes
• Dozens more in evaluation

Most broadly available
• Portable to any process
• 180nm > 3nm and 18A
• 1K > 2M LUT capacity
Applications adopting eFPGA

- Communications
- Wireless
- High Performance Compute
- Automotive
- Healthcare
- Defense
Some of Our Customers

High-Volume Commercial

- Renesas
- Socionext
- Alphawave
- DTT

Most of our new evaluations are high volume commercial customers

Major 5G
Major Fintech
Major Storage

US Government

- Sandia National Laboratories
- U.S. Department of Defense
- AFRL
- Boeing
- DARPA

Major Prime Contractors
eFPGA is strategically important for the US Government: developing for US Fabs at 90/12/5/3/1.8nm
Renesas ForgeFPGA Family – 1K, 2K, 4K, 8K LUTs

Renesas Unveils Ultra-Low-Power, Low-Cost ForgeFPGA™ Family

- TSMC 40nm eFPGA
- EFLX Compiler
- <50 cents in volume
5G Solution: 100K LUTs @ 500MHz+ SS/125C on N7

• High performance architecture in development
• Integrated system solution replacing traditional FPGAs like Xilinx and Achronix
• Deployment across dozens of customers and applications
• 5G performance and scalable solution
eFPGA for Flexible GPIO in MCUs and SoCs

• There are dozens of flavors of common GPIO like UARTs and SPIs
• Before you could integrate as many flavors as possible OR make your customers use FPGAs to couple to their flavor of UART/SPI
• Now you can use eFPGA to enable ANY GPIO function to be programmed so customers get exactly what they want and system cost is reduced
eFPGA Available in Many Sizes with Many Options

- eFPGA sizes 1K to >2M LUTs

- EFLX Tiles
  - Regular FPGA has Logic/MACs/RAM
  - We give you only what you need

- Delivery time
  - EFLX is Hard IP for best PPA
  - Uses Foundry Standard Cells
  - Weeks on a supported process and node
  - Months on a new process or node

Largest Array Delivered So Far: 12nm, 240K LUTs, 12x9 mm
Growing EFLX Ecosystem

RTL IP Companies

ASIC and Design Services

Synthesis Tools

Foundry
FPGA Integration into your SoC cuts power & cost 5-10x

Major power and cost reduction

<table>
<thead>
<tr>
<th>Description</th>
<th>Cost Saving</th>
<th>Power Saving</th>
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<tbody>
<tr>
<td>No FPGA margin</td>
<td>60%</td>
<td></td>
</tr>
<tr>
<td>No FPGA package, reduce PCB area, voltage converters</td>
<td>15%</td>
<td>10%</td>
</tr>
<tr>
<td>Remove</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• SERDES/DDR/IO</td>
<td>15%</td>
<td>75%</td>
</tr>
<tr>
<td>• Unused blocks of the FPGA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Harden unchanging FPGA logic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>90%</td>
<td>85%</td>
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Smaller, Faster XFLX™ Interconnect Technology

Designed for IP Integration

• Xilinx performance with ½ the transistors and ½ the metal layers
• Best metal stack compatibility for easy integration
  • 5nm 9 layers, 16nm 7 layers, 28nm 6 layers, 40nm 5 layers
EFLX Array Features and Size

• Basic building block is an EFLX™ tile
  • 3 major tile architectures

• Each tile has a top-level interconnect, ArrayLinx™
  • Thousands of wires on each edge

• Tunable for minimum power or maximum performance

• EFLX cores connect via abutment
  • Array-level mesh interconnect connected with no GDS changes

• Timing is done at the array level in days for all process corners

Available EFLX Tiles

- Logic
- Logic + DSP
- Logic + IO
- EFLX 1K LGC
- EFLX 1K DSP
- EFLX 4K LGC
- EFLX 4K DSP
- EFLX 4K IO
Arrays optimized for the size and compute mix you need

- From 1K to >1M LUTs; DSP, max-IO and RAM options
- Array is built and delivered by Flex Logix with corner timing and Compiler
• Put SRAM (BRAM) in an EFLX array
• Our standard RAM is configurable
  • Single, 2 or true dual port
  • 32x1K or 16x2K or 8x4K or 4x8K
• We can handle other types of SRAM like ECC but engineering effort is greater
• EFLX Compiler maps your RTL onto the array including the SRAM
• MBIST ports output to SOC level
EFLX Pass-through option for routing through large EFLX Arrays

- Route critical chip level signals through the EFLX array
- Reduces chip level complexity
  - Place and route
  - Signal routing
  - Timing closure
- Provides dedicated North-South and East-West paths
- Minimizes overhead using EFLX array in large high-density designs
Rapidly Reconfigurable eFPGA

• Traditional FPGA is loaded at boot and never changed
• eFPGA can be reconfigurable
• Configuration bits can be streamed from DRAM or SRAM cache for millisecond reconfiguration
• A special cache RAM can hold configuration bits for microsecond reconfiguration
• This enables workloads to be switched dynamically
• Traditional FPGA is one large Verilog program: any change to code causes place-and-route to be redone often with significant timing variation

• Instead with SW-FPGA:
  1. One block of eFPGA runs independently of others and runs the same in any location
  2. Host processor “calls” eFPGA like a subroutine
  3. This can be configured once at run-time or, using the rapidly reconfigurable option, can be updated one block at a time in milliseconds or microseconds
Mix and Match As Needed for the Application – tiles run separately OR can be run as larger array for bigger code

Configure at boot time

OR

Re-configure dynamically as workloads shift
Use eFPGA for Control Path with Hardware ASIC Blocks

- Achieves the flexibility and adaptability of eFPGA for changing requirements
- Density and performance much better than if compute is in FPGA
- See in the next section how we do this for AI and DSP
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| Achronix | - Must use their metal stack and maximum metal layers  
|         | - Less granularity, options                                  |
|         | - Only TSMC 16/7                                             |
| Menta  | - 2x more area                                               |
|         | - Can’t do larger arrays                                     |