Top 5 predictions for eFPGA in 2022

By Andy Jaros

With the eFPGA now readily available in many process nodes from multiple suppliers, Flex Logix offers predictions on what we can expect to see around eFPGA development and use cases in 2022 and beyond.

The need for reconfigurability in systems on chip (SoCs) will continue to increase in 2022 along with the rapidly rising cost of developing SoCs especially at advanced process nodes. As prices increase, so does the pressure for SoC providers to generate a lot of revenue on their products. This can be possible if reconfigurability allows the SoC to be used in a wider range of applications. The embedded FPGA (eFPGA) approach can deliver that flexibility.

In the past, eFPGA was typically not the first intellectual property (IP) a chip architect would consider for a project. After all, there have been hundreds of thousands, if not millions, of chips designed without it. However, that mindset has been steadily changing and the most significant reason now is because customer requirements are more demanding.

They need more performance *and* lower power and at the same time, the cost and design cycles for chip development continues to skyrocket. These constantly changing demands require a changeable solution.

With the eFPGA now readily available in many process nodes from multiple suppliers, here are our predictions on what we can expect to see around eFPGA development and use cases over the next year and beyond.

5G ASICs lead eFPGA adoption

5G, and more specifically, open RAN, is a perfect application for eFPGA. Integrating eFPGA in an ASIC can address high compute demands needed for massive MIMO and packet processing. It can do this while retaining the low power and weight benefits of an ASIC with the ability to customize the hardware in support of RU and DU interoperability, regional, carrier or site-specific requirements.

Large FPGA users develop their own FPGA platforms

We've seen this play out before. Qualcomm, Apple, Broadcom, Marvell, Microsoft, have all taken Arm architecture licenses to create Arm implementations specific to their needs that they could not get from Arm.

Meanwhile, Apple, Amazon, Facebook, Microsoft, have applied the same concept to ASIC development because they need to control both their hardware and software development and roadmaps. The same process will play out for large FPGA users who really need a customized FPGA using eFPGA to execute changing workloads in support of their products and services roadmaps.

More systems companies seek eFPGA from MCU / ASSP suppliers

When does Moore's law end? Who knows? There are many very smart physicists and process engineers working on that problem. For some, though, it ended at 55nm or 40nm because of cost and leakage power reasons. A common choice to add compute power at the most advanced nodes or squeezing more power on any given node is to use purpose-built accelerators.

Many systems companies already use FPGAs to provide additional compute resources ranging from high powered Xilinx FPGAs for networking applications down to small, low-powered FPGAs from Renesas or Lattice for battery and IoT devices. As companies get more reliant on FPGA flexibility, they will seek and ask for eFPGA functionality on their SoC, ASSP or MCUs.

FPGA to ASIC conversion picks up steam

It's always been a tug of war between the continued use of using expensive FPGAs in a product versus committing to pay ASIC development fees and recouping them through lower ASIC chip costs. One of the drawbacks to converting an FPGA to ASIC is that once the ASIC is done, the only way to change it is to re-tape it out again.

eFPGA changes that equation. Retaining reconfigurability in key parts of the design provides a path to upgradability, bug fixes and new functionality that extends the useful lifetime of the chip. A longer lifetime equals higher volumes, which equals cost justification to convert to ASIC. The net result is lower chip cost and higher system margins.

Security will benefit from eFPGA reconfigurability

Security covers a wide span of use cases including root of trust, encryption, side channel attack protection, and design obfuscation. Threats targeting embedded systems are ever increasing, getting more sophisticated and constantly changing. Security solutions will need to change over time, too.

It's well documented that it's just a matter of time before quantum computers will be able to crack encryption algorithms that are hard wired in today's chips within hours. Having the ability to update security circuits in a deployed system to stay a step ahead of hackers has tremendous value to companies. More clever solutions could also leverage the temporal aspect of dynamically reconfiguring the eFPGA in situ. With eFPGA now broadly available, security architects can leverage dynamically reconfiguring circuits post tape-out, to come up with unique and novel security solutions.

These are just a few of the predictions we see for eFPGA in the coming year. Long considered a holy grail of chip design, eFPGA has finally made its way into the mainstream and is going to be playing a significant role in the future development of chips. It's going to be fun to watch.

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