InferX™ DSP IP & SW
World Class DSP in your SoC

flexlogix® reconfigurable

Fast streaming DSP at low cost and low power for your SoC

- ✔ 80% hardwired, 100% reconfigurable - as flexible as FPGA but less $/W/size
- ✔ InferX tile (N5): 2 TeraMACs/second (INT16, INT40 accumulate); N tiles = N x faster
- ✔ 10x cheaper, 10x lower power and much smaller than using FPGAs
- ✔ Fully reconfigurable in microseconds for any DSP operation (and even AI Inference)
- ✔ TSMC 16, 7, 5 and 3nm nodes
- ✔ We do the coding: softlogic available for FFT, FIR, matrix inversions, etc.
- ✔ AXI bus interface to your SoC
- ✔ -40 to +125C Tj.
- ✔ High DFT test coverage both DC and AC for high quality test
- ✔ Dozens of chips have worked first time with our IP and Software

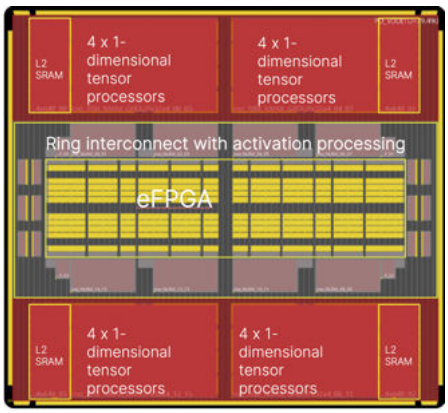
TSMC IP Alliance Member

Flex Logix® is a TSMC IP Alliance Member based on the work it has done with TSMC over many years to develop IP meeting TSMC9000 compliance for design methodology, validation in silicon & documentation. Flex Logix has implemented IP in TSMC 40, 28, 16, 12 and 7nm; and has started on 5nm. Dozens of customer chips are working in silicon with our IP; dozens more are in design.

InferX Hardware

InferX is a compute tile, as shown right.. InferX uses eFPGA for programmable state machine control of 16 one-dimensional tensor processors that are connected with programmable interconnect. This allows configuraiton of the hardware for optimal execution of a given DSP task. It is reconfigurable in microseconds.

InferX is delivered as a single tile or an array as large as needed for your performance requirement.
InferX performance is linear: An array with N tiles will run about N times faster than a single tile array.
The array has an AXI bus interface to connect to your SoC. An 8 tile array, organized as 2x4, is shown below.



Selected DSP Benchmarks in N5

Operation	1 InferX Tile TSMC N5	8 InferX Tiles TSMC N5
Complex INT16 1K/2K/4K FFT	8.5 GS/s (Gigasamples/sec)	68 GS/s
Real INT16x16 FIR 256 taps	4 GS/s	32 GS/s
Real INT16x16 FIR 4096 taps	0.25 GS/s	2 GS/s
32x32 Complex INT16 Matrix Inversion	0.2M/sec	2.6M/sec
Area (est.)	5.5 mm²	44 mm2
Typical power (est) TT/25C Tj	1 W	8 W