TSMC 40ULP EFLX® 1K eFPGA Tile: Silicon Proven

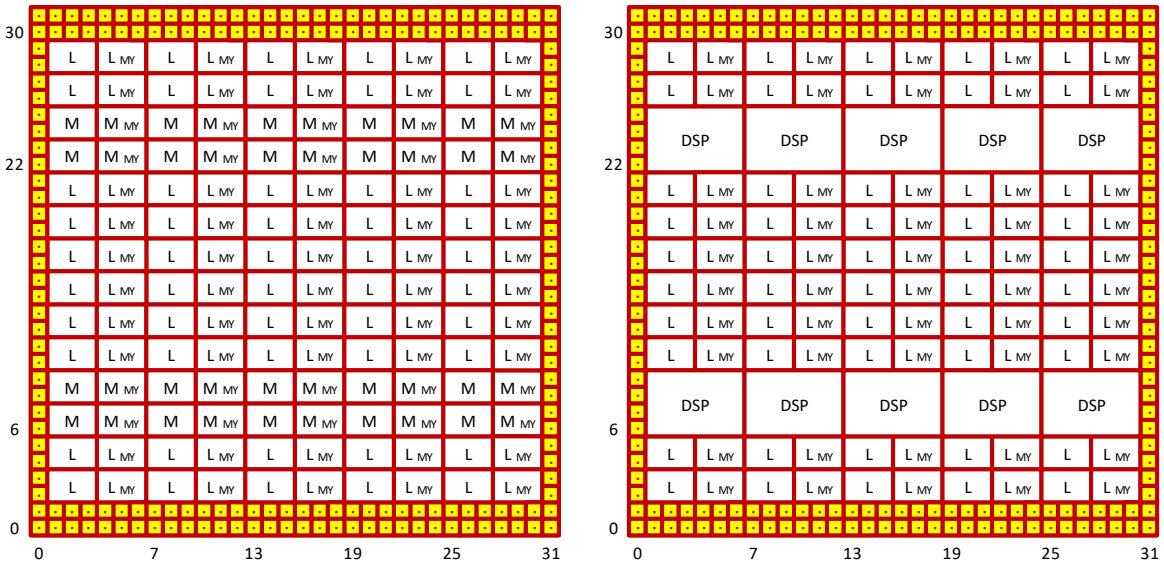
The EFLX® 1K Logic IP tile is an eFPGA (embeddable FPGA) IP tile **with power management** containing 560 Look-Up-Tables (LUTs: each is 6-input, or dual-5-input, with 2 independent outputs with 2 bypassable flip flops) and 5 Kbit RAM, Gen 2.0 XFLX™ interconnect network, multiple clocks & scan: fully reconfigurable in-field at any time. The EFLX 1K Logic tile is silicon proven. EFLX 1K DSP tile is "on demand".

The EFLX 1K DSP tile has 10 DSP MACs (22x22 multiplier with 48 bit accumulator).

EFLX tiles can be arrayed to create larger arrays. Logic and DSP tiles can be mixed. And RAM can be integrated as well.

EFLX features full connectivity inside the tile, and provides ArrayLinx interconnects at the boundary to concatenate multiple tiles via the expandable network I/Os.

Name	EFLX® 1K Tile Gen 2.0	
Technology	TSMC 40ULP	
Metal Stack	M1+ 5X1Z Top IP Layer : MZ (M7)	
Nominal Supply Voltages (Vj)	1.1 V	
Junction Temperature (°C)	−40 to 125	
Leakage Power	0.03 mW @ TT, 1.1V, 25C Tj	
Clocks	2/tile, N tiles = 2N clocks	
Area (mm^2)	1.5 mm^2	
Input and Output Pins	368 input & 368 output, each with an optional flip-flop	
Look-up Tables (6-input LUT with two independent outputs)	Logic/Mem Tile	DSP Tile
	560 (~900 LUT4)	400 (~650 LUT4)
Distributed Memory (Kb)	5 Kbits	0 Kbits
22-bit DSP MACs	0	10
EFLX Array Sizes Possible	1×1 to >4x4	
Design-for-Test Support	Yes, fault coverage under NDA	



The EFLX 1K tile has 368 input pins and 368 output pins. The I/O pins provide user access to the EFLX tile. Each I/O has a bypassable flip flop. When multiple tiles are concatenated into EFLX arrays, the user I/Os along the abutting edges are disabled (or are used for controlling embedded RAM blocks).

flexlogix® reconfigurable

Besides input/output pins, there are clock, configuration, and test/DFT pins. Each tile has an internal power grid which can be connected to the customer's digital SoC power grid. The tile has power control pins. The tile also has configuration ports to load the bitstream. An AXI or JTAG interface is available for configuration. A clock mesh provides multiple connect points.

Readback circuitry in Gen 2.0 enables configuration bits to be read back anytime to enable checking for soft errors to improve reliability for high-reliability applications. A new test mode enables test times about 100x faster to lower test costs.

Deliverables and EDA Design Views: Available Now for EFLX 1K Logic Tile in TSMC 40ULP/LP	
Front-end Design view (with NDA)	**Back-end Design Views (with License)**
Encrypted Verilog Netlist	Encrypted Verilog Netlist with Timing Annotation & SDF
LIB	GDS-II
Footprint LEF	CDL/Spice netlist
Detailed datasheet & DSP User's Guide	Integration guidelines & assistance
EFLX Compiler evaluation version	Test Vectors for DFT fault coverage
	EFLX Compiler bitstream generation version

Power Management

The eFPGA tile operates in one of two modes

- Dynamic: full speed operation
- Sleep: VDDH on, VDDL gated; configuration, flip-flop and RAM states retained

Power gating the bulk of circuitry allows the minimum sleep power to be much lower but reduces the voltage budget for that circuitry which also reduces maximum frequency operation.

EFLX for TSMC 40ULP/LP is power-gated because customers in this node prefer this tradeoff.