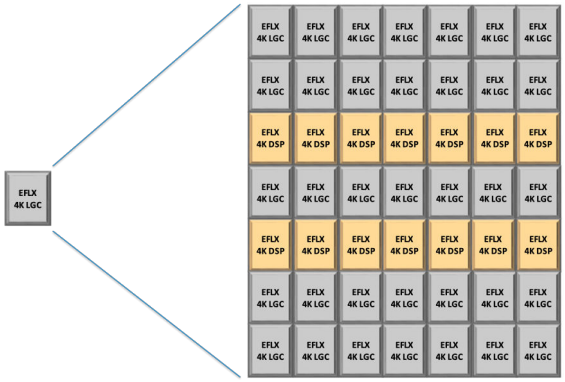
# TSMC 3/4/5/6/7/12/16/28/40nm EFLX®4K eFPGA Tiles

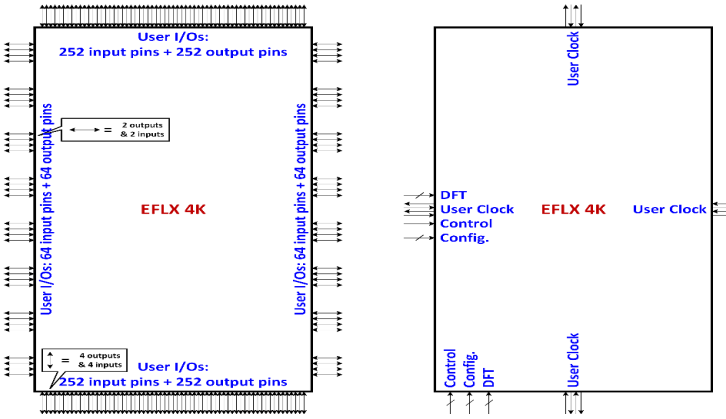
The EFLX®4K Tile is an embeddable standalone FPGA IP core, with 2 versions, that communicates with the rest of your SoC using input and output pins on the edges. For more logic capacity we can abut tiles to make larger arrays (up to ~8x8) with any combination of tile versions.

The two versions of the EFLX tile are described below – they are all the same dimensions so they can be intermixed in arrays. The DSP MAC is a 22x22 multiplier with 48-bit accumulator arranged in 4 row of 10 pipelined MACs.




| EFLX 4K Versions: | **EFLX 4K Logic Tile** | **EFLX 4K DSP Tile** |
|---|---|---|
| Clock Inputs | Gen2.4 has 8 clocks/tile (4 unique & their inverses) = 8N for N-tiles.<br>Gen 2.0/2.2 has 2 clocks/tile. | |
| Look-upTables<br>(6-input LUT with 2 independent outputs) | 2,520<br>(~4.0K LUT4) | 1,880<br>(~3.0K LUT4) |
| Total Flips Flops (ex DSP MACs) | 6,304 | 5,024 |
| Distributed Memory | 21 Kbits | 1 Kbits |
| 22-bit DSP MACs | 0 | 40 |
| I/O Pins, with optional flip flop | 632 input & 632 output | |

The EFLX 4K tiles have numerous input and output pins. Each input or output pin has a by-passable flip flop. When multiple cores are concatenated into EFLX arrays, the pins along the abutting edges are disabled or are used for controlling embedded RAM blocks (BRAMs).




*EFLX 4K Logic/DSP input/output map (IO tile has more IO top+bottom)*

Besides input/output pins, there are clock, configuration, and test/DFT pins. Each Core has an internal power grid which can be connected to the customer's digital SoC power grid. The Core also has configuration inputs on the West side and configuration inputs on the South side to load the bitstream. An AXI or JTAG interface is available for configuration. A clock mesh provides multiple connection points. The configuration bits can be read back anytime to enable checking for soft errors to improve reliability for high-reliability applications.



flexlogix reconfigurable

| Node | **N5/4 & N3** | **N6/7** | **N16/12 FFC/FFC+** | **N16/12 FFC/FFC+ Low Power** | **N28 HPC/HPC+** | **40LP** |
|---|---|---|---|---|---|---|
| EFLX Generation | 3.0 | 2.2 | 2.0 | 2.4 | 2.0 | 2.4 |
| Clocks | 8/tile, 8N for N-tile array | 2/tile, 2N for N-tile array | 2/tile, 2N for N-tile array | 8/tile, 8N for N-tile array | 2/tile, 2N for N-tile array | 8/tile, 8N for N-tile array |
| Metal Stack | Under NDA | M1+1X1Xa1Ya5Y IP Top Layer: My (M9) | M1+2Xa_1Xd_h_3Xe IP Top Layer: MXe (M7) | M1+2Xa_1Xd_h_3Xe IP Top Layer: MXe (M7) | M1+5X IP Top Layer: MX (M6) | M1+5MX+MZ IP Top Layer: MZ (M7) |
| Nominal Supply Voltages (Vj) | Under NDA | 0.65, 0.75, 0.85 | 0.55, 0.75, 0.8, 0.85, 1.0 | 0.55, 0.75, 0.8, 0.85, 1.0 | 0.8, 0.9 | 1.1 |
| Temperature Range (Tj) | -40 to +125 | -40 to +125 | -40 to +125 | -40 to +125 | -40 to +125 | -40 to +125 |
| Availability | In development | Available | Silicon proven | In development | Silicon proven | In development |
| Leakage Power | Under NDA | 6.8 mW (N7, TT, 0.7Vj, 25C Tj) | 3.4 mW (16FFC, TT, 0.8Vj, 25C Tj) | Under NDA | 1.9 mW (HPC+, TT, 0.9Vj, 25C Tj) | Available soon |
| Area ($mm^2$) | Under NDA | 0.65 | 1.0 | Under NDA | 1.6 | 6.9 |

Evaluation Licenses are available free for you to try your RTL on our EFLX Compiler for your node/array size/features to check performance: timing is available for multiple process corners.

When you integrate ELFX eFPGA into your SoC/ASIC, our engineering team will work closely with you. We have a detailed architectural specification and numerous deliverables. We help you with design, DFT and production test. We are with you all the way through production ramp.

We are constantly improving DFT coverage. For Gen 2.4 Stuck-at (DC) is >98% and transition (AC) is >95%.

| **Deliverables and EDA Design Views** | |
|---|---|
| **Front-end Design view (with NDA)** | **Back-end Design Views (with License)** |
| Encrypted Verilog Netlist | Encrypted Verilog Netlist with Timing Annotation & SDF |
| LIB | GDS-II |
| Footprint LEF | CDL/Spice netlist |
| Detailed datasheet & DSP User's Guide | Integration guidelines & assistance |
| Silicon validation report available | Test Vectors for DFT test coverage |
| EFLX Compiler evaluation version | EFLX Compiler bitstream generation version |

Evaluation boards are available for some process nodes.