# EFLX® Embedded FPGA
## #1 Supplier Proven in >25 Chips

flexlogix® reconfigurable

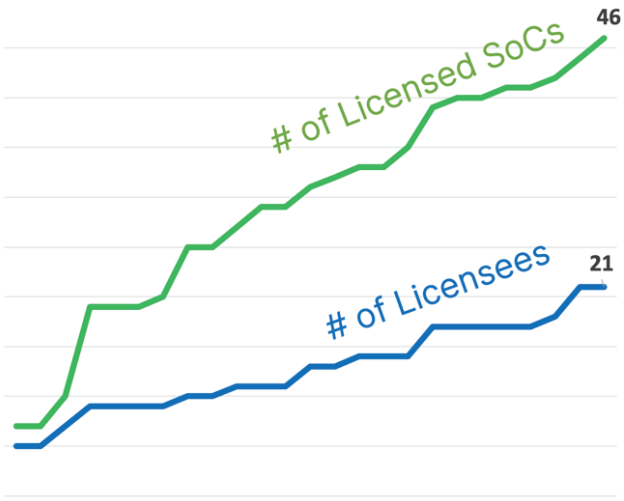
## eFPGA Adoption is Accelerating!

eFPGA allows you to expand your market, extend your chip life, avoid mask spins, and accelerate parallel work loads.

Customers select Flex Logix EFLX because we support the most nodes, we have the best PPA and we have the largest market share.

>25 Chips with EFLX eFPGA have fabricated successfully. Dozens more are in design across multiple process nodes and multiple applications.

Customers include Renesas, Boeing, Datang Telecom, Sandia National Labs, DARPA, DoD, AFRL & many more not yet public. ASIC companies with eFPGA experience include Socionext, GUC, Alphawave and Synapse. Several customers have used eFPGA in their Chiplets.




## Wide Range of Market Segments

## eFPGA: Benefits of Integration

### Save Money
Reduce Mask Spins and save engineering cost by moving risky IP to programmable logic

### Extend Product Life
Adapt to new interfaces and protocols. Evolve with emerging algorithms and security threats

### Expand Market
Interface flexibility to meet unique market and regional requirements

### Enable Differentiation
Flexibility and adaptability to enable unique features vs competition

### Support Changing Workloads
Context aware Programmable data planes enable algorithms to adapt to incoming data

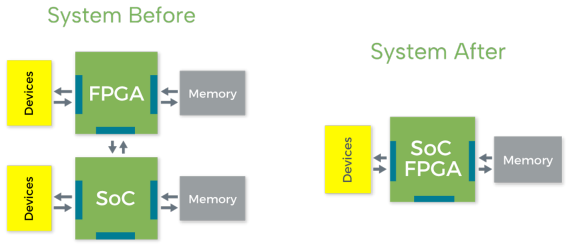
### Accelerate Computation
Parallel and pipelined processing accelerates complex algorithms and enables determinism

# EFLX eFPGA Use Cases

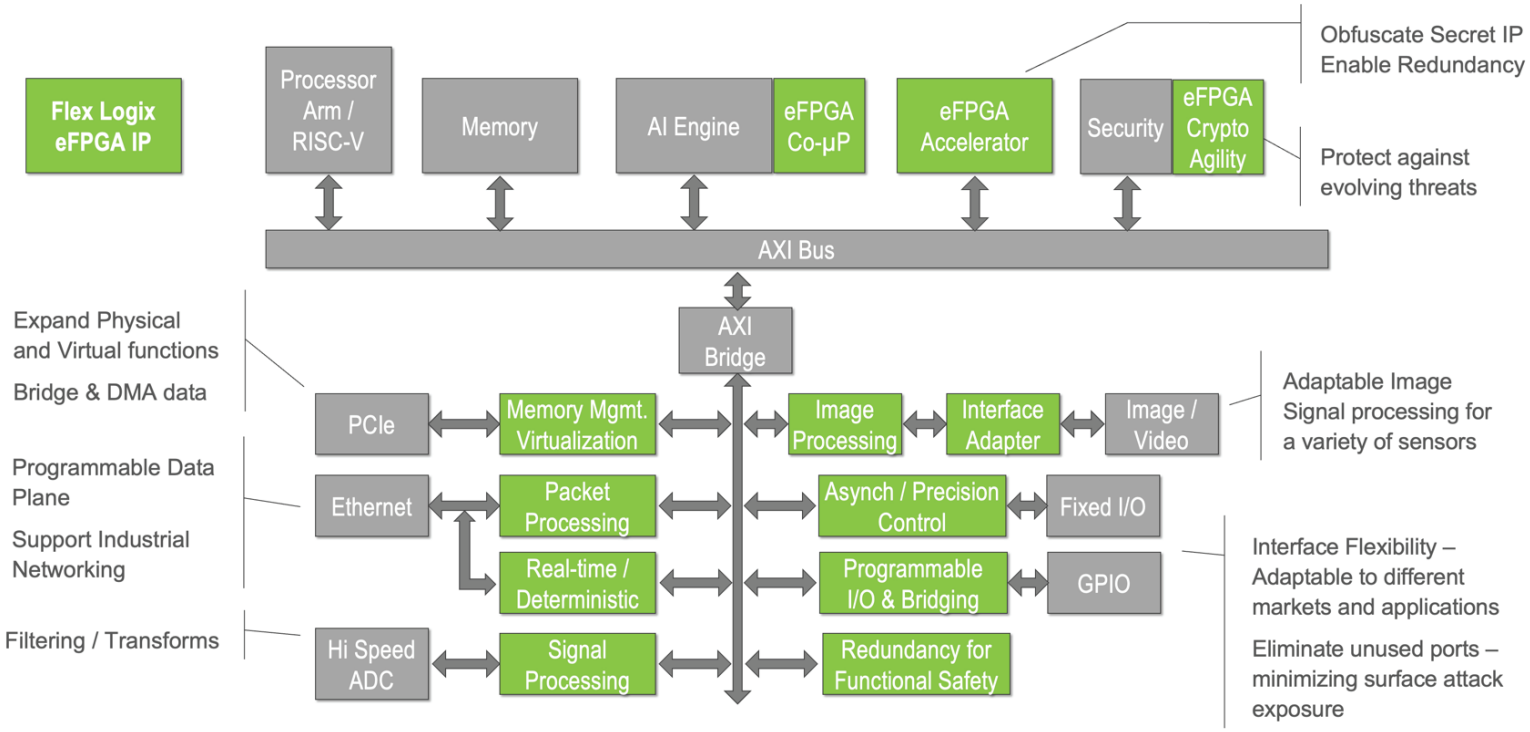
## Adapt to changing standards, algorithms, market needs

## Cut FPGA power/cost 10x by integration

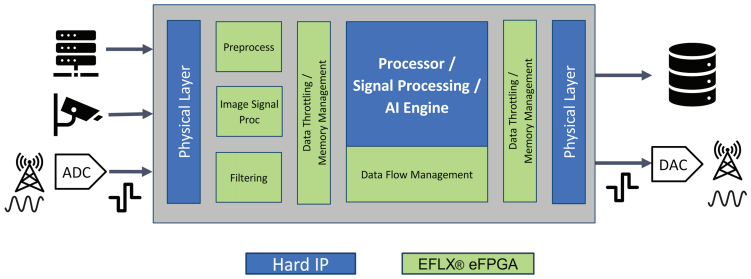
FPGAs are used in virtually every type of system. As volumes grow customers want to cut FPGA cost and power: by integrating eFPGA into their SoC they can cut 90% of the FPGA cost and 90% of the FPGA power. Also they replace 2 packages with 1 saving board space and expensive voltage regulators.The SoC+eFPGA is just as fast and just as programmable.




## eFPGA in an SoC has dozens of use cases to add value




## eFPGA pre/post processing for AI/DSP




## Renesas ForgeFPGA: small, low power

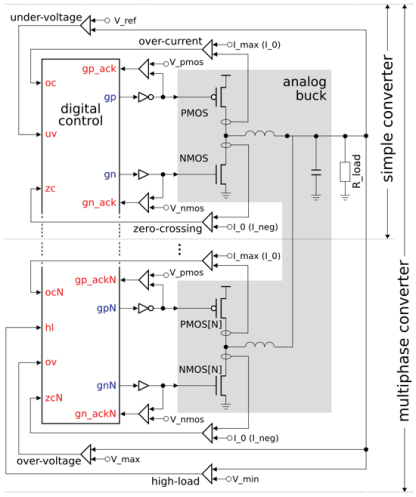
Renesas' Forge FPGA family is based on Flex Logix 40ULP EFLX eFPGA starting at 1K LUTs and is programmed with EFLX Compiler.

ForgeFPGA is the smallest, lowest power, lowest cost FPGA on the market starting at just a couple millimeters on a side.

## Reconfigurable Asynchronous Control

Replace hardwired asynchronous digital control with 200 LUTs of asynchronous programmable logic

- reprogram any time
- adapt to chang-ing specs
- experiment with new algorithms
- program using Workcraft
- timing checked for all PVT corners




Workcraft

# EFLX eFPGA Software
## All the tools you need

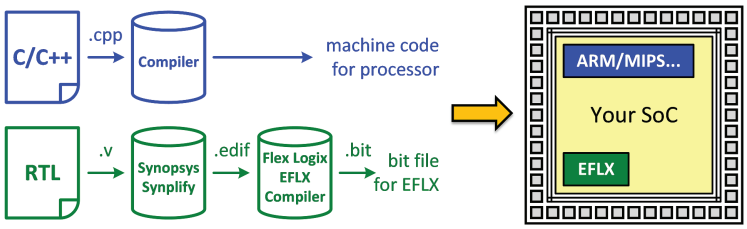
flexlogix reconfigurable ®

## Proven EFLX Compiler Software

The EFLX Compiler has been in use by dozens of customers for years. We use Synplify for synthesis the same as many large FPGA companies.

It's easy to use.

We can give you a free software evaluation license for the process node you are targeting to determine area, speed and power of your RTL.




## eXpreso™ is coming in 2024: Faster runs, higher frequency, more LUTs

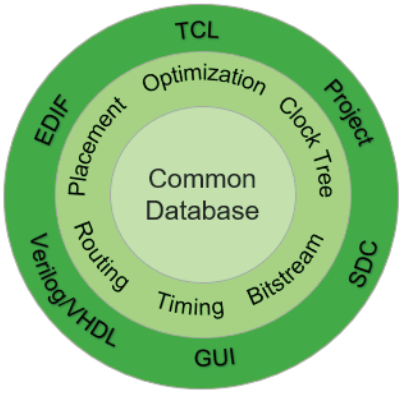
eXpreso EFLX Compiler is our 2nd generation compiler. Beta evaluation will be available for some nodes in Q2. Full release in 2H 2024 for all nodes.

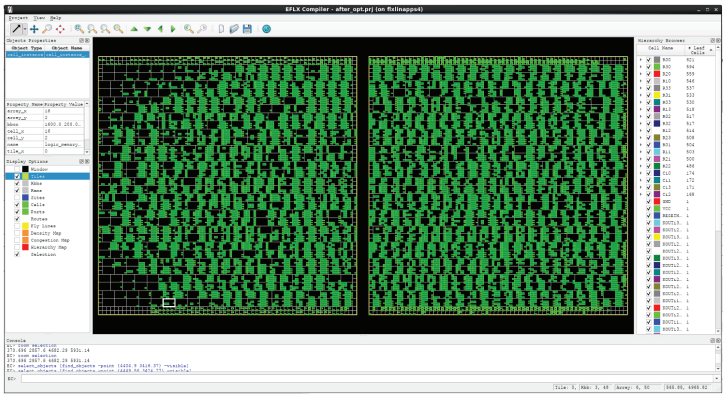
eXpreso leverages our years of experience with customer designs and modern EDA techniques to deliver much better results.

Compile times are up to 10 times faster.

Frequency is up to 50% higher.

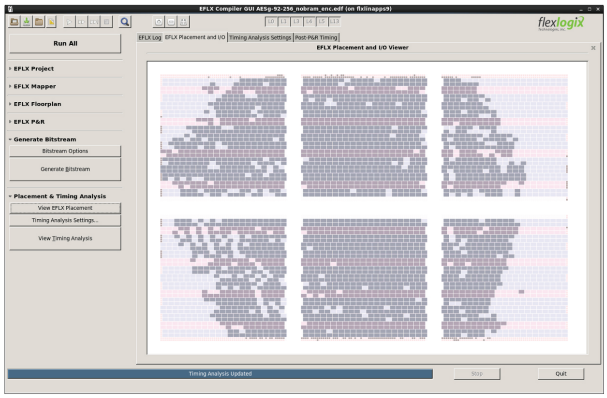
And up to 2x more LUTs are packed into the same silicon area. Below are several designs compiled on eXpreso vs EFLX Compiler 1.0. The increase in packing density comes with higher frequencies.



**eXpreso 2 tiles**

**AES256**



**EFLX Compiler 1.0 6 tiles**

## Crypto Agility: Reconfigurable algorithms for Post Quantum Security

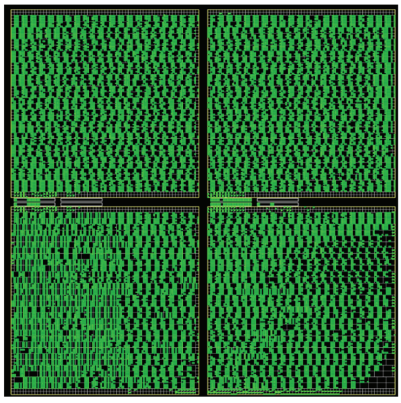
Keep keys in eFPGA for reconfigurability and safety.

Use Post Quantum cryptography algorithms in reconfigurable logic to update them as they are improved over time.

Xipher's ML-KEM (Kyber) runs 1.8GB/sec in 2.6 mm2 of N7.

### ML-KEM Implementation Example

- IP fits compactly into 2x2 EFLX4K Tile Array with > 90% utilization
  - 10K LUTs | 5K Registers | 8 BRAMs
  - Can be implemented on any ASIC or SoC on any technology node
- Fast 225MHz clock rate (typical, TSMC 7nm)

*Flex Logix EFLX 4K Tiles*

# EFLX eFPGA Hardware

## eFPGA 180nm to 18A: fast, dense, your metal stack

## We are IP Alliance Members with Intel, TSMC, GF

| | | |
|---|---|---|
| Intel 18A | EFLX 4K | Design starting Q2/24 |
| TSMC N3 | EFLX 4K | In design: PPA under NDA |
| TSMC N5/N4 | EFLX 4K | In design: PPA under NDA |
| TSMC N7/N6 | EFLX 4K | Available - delivered to lead customer |
| TSMC 12FFC/+/16FFC/+ | EFLX 4K | PROVEN IN SILICON |
| TSMC 12FFC/+/16FFC/+ | EFLX 4K Low Power | In design; PPA under NDA |
| TSMC 28HPC/HPC+ | EFLX 4K | PROVEN IN SILICON |
| TSMC 40ULP | EFLX 1K | PROVEN IN SILICON |
| TSMC 40LP | EFLX 4K | Available - delivered to lead customer |
| GlobalFoundries 12LP/12LP+ | EFLX 4K | PROVEN IN SILICON |
| GlobalFoundries 12LP/12LP+ | EFLX 4K RHBD | PROVEN IN SILICON |
| GlobalFoundries 22FDX | EFLX4K | Available - delivered to lead customer |
| Sandia 180 | EFLX4K RH | PROVEN IN SILICON |

Detailed product briefs are available for each EFLX core. Operating temperature range is -40C to +125C Tj.

## #1 PPA eFPGA compatible with most metal stacks

EFLX eFPGA has density and performance similar to Xilinx in the same node. Because of our patent interconnect technology, we achieve this with many fewer metal layers than traditional FPGA so we are compatible with most metal stacks. Two of our competitors are 2-4x more area/power for the same number of LUTs/MACs/RAM. Another competitor has similar density but is only available for 2 nodes compared to our 12 nodes including N5/4/3 + Intel 18A.

## Get exactly the eFPGA you want using our modular architecture

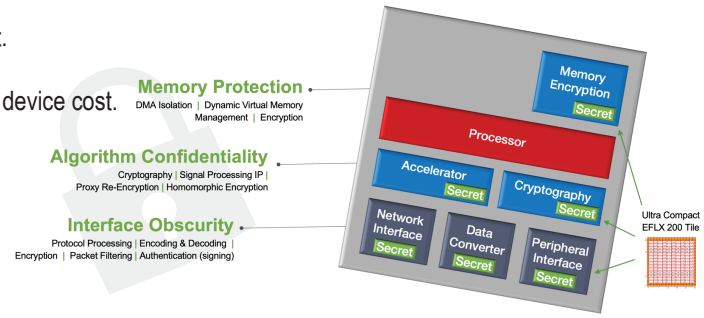
LUTs from 1 Thousand to >1 Million. Glitchless LUT option for Asynchronous operation with EFLX Compiler timing support
No MACs or lots of MACs. BRAM from none to as much as you need with parity and ECC options. Clocks from one to dozens.
AXI bus interface to the rest of the array or thousands of pins for direct control.

## High volume reliability and test features

DFT >98% stuck-at and >90% transition. Roadmap for Automotive >99% stuck-at.
MBIST port for SoC control of BRAM MBIST and repair.
High speed test modes and low pin count test modes to minimize production and device cost.

## Tiny EFLX-200: just 0.04mm² in N5

We can provide a very small eFPGA in any TSMC process node: Obfuscation, reprogrammable state machines & asynchronous programmable logic.




## Emulation support for first time silicon success

We support emulation models for EFLX Arrays, for exactly the size and features you specify, for Siemens Veloce and Cadence Palladium systems. These emulations models have been used extensively in development of customer SoCs to ensure right-the-first-time silicon.

## EFLX Generation 3.0 for Advanced Nodes: N5/3/4 & 18A

Several new features are being introduced with Gen 3.0 for N5/4, N3 and 18A:

- improved interconnect for long routes enabling >1 Million LUTs in combination with Xpresso EFLX Compiler
- pipelined interconnect enabling higher frequency soft logic operation
- LUTs that can be programmably used as IO's for applications that require thousands of control pins per tile such as InferX DSP/AI

**www.flex-logix.com**