NEWS RELEASE

FLEX LOGIX EXTENDS EMBEDDED FPGA-IN-SOC ARCHITECTURE WITH NEW BLOCK RAM AND DSP CORES

Addition of Popular FPGA Features Addresses Even Wider Range of Applications

Santa Clara, CA (17 September 2015)—Flex Logix, innovative developer of FPGA-in-SoC technology, today announced the extension of its core FPGA logic architecture to include Block RAM (BRAM) and DSP cores. Both BRAM and DSP are popular extensions found in traditional stand-alone FPGA products. The addition of low-latency memory and signal processing capabilities significantly increases the range of applications addressed by Flex Logix' EFLX™ embedded FPGA-in-SoC architecture.

Flex Logix' EFLX technology allows system-on-chip (SoC) designers to embed field programmable gate arrays (FPGA) into complex chip designs. The inclusion of FPGAs into a SoC enables key functions to be optimized or customized after the device is completely fabricated—even updating logic after a device is installed into a system in the field.

By adding BRAM and DSP, Flex Logix expands the tool kit available to designers for this post-production flexibility. For instance, applications such as encryption, networking and signal processing require blocks of RAM to be integrated into the FPGA to provide fast local memory to implement buffers, scratchpads, FIFOs, and other low-latency memory that improves performance.

While traditional FPGAs typically offer one type and size of RAM that can "emulate" different widths, Flex Logix' Block RAM architecture can provide exactly the type and amount of memory an application requires. This flexibility is accomplished by inserting BRAM between the EFLX logic cores—which "tile" together to make an array—controlling them with otherwise unused inward-facing inter-tile I/Os. Flex Logix can support single-port RAM or dual-port RAM, any width, any amount; ECC, parity or no error checking; even MBIST—offering far more flexibility than available in traditional stand-alone FPGA chips.

EFLX DSP Cores Accelerate Signal Processing

In addition to local memory, many applications also require digital signal processing (DSP) capability. Wireless base station digital front ends, image and audio processing, and other applications require high-performance DSP functions such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transforms (FFT).

The basic building block for implementing these DSP functions is a pre-adder/multiplier/accumulator (MAC). Flex Logix now offers an EFLX Logic core that incorporates 40 MACs with 22-bit inputs and 48-bit accumulation. The MACs can be combined for 2x precision and pipelined for high throughput. They can also be used as complex-number MACs for certain DSP algorithms.

Performance specs for a single Flex Logix' DSP core are similar to that of existing stand-alone 28nm FPGA chips, achieving 500 Msamples/second for a 22-bit 5-tap FIR and 300 Msamples/second for a 22-bit 40-tap FIR. Multiple EFLX DSP cores can be combined to implement more complex DSP functions.

Development Software Evaluation Licenses Now Available

The EFLX Compiler maps standard Verilog/RTL into the EFLX array, including DSP and Block RAM (and even including external Block RAM if desired). Customers do not require any FPGA expertise to use Flex Logix technology.

The silicon-proven EFLX Compiler has been in use at customers for several months.

Flex Logix is now offering evaluation licenses so qualified customers can test the software at their offices: contact Flex Logix to inquire about an evaluation license.

TSMC OPEN INNOVATION PLATFORM September 17, 2015

Flex Logix has been selected to demonstrate its technology at the TSMC Open Innovation Platform Ecosystem Forum, September 17, at the Santa Clara Convention Center, Booth #405. Flex Logix will disclose more details and application information on its new BRAM and DSP cores, and the EFLX software evaluation kit.

Product Availability & Pricing

The new EFLX BRAM and DSP cores are available now. Silicon validation has been completed in TSMC's mainstream 28nm process.

Depending on the number and size of EFLX logic, BRAM and DSP cores incorporated into a SoC design, the incremental manufacturing and licensing cost is expected to be less than 5 cents per thousand LUTs.

About Flex Logix

Privately held Flex Logix licenses its patented EFLX technology that enables FPGAs to be embedded into SoCs. This capability dramatically reduces manufacturing and design risk, enhances development flexibility, and accelerates technology roadmaps for a wide array of applications by allowing system designs to be updated after initial manufacture.

The company is led by co-founder and CEO Geoff Tate, the founding CEO of IP licensing pioneer Rambus. Flex Logix co-founders include Dr. Cheng C. Wang, Dr. Fang-Li Yuan and UCLA professor of electrical engineering Dr. Dejan Markovic, who received the prestigious 2014 Lewis Award for Outstanding Paper at the International Solid State Circuits Conference (ISSCC), for their description of the concepts embodied in EFLX.

Contact Flex Logix at info@flex-logix.com or see our website www.flex-logix.com.

####

Media Contact:
Spencer Horowitz
PR for Flex Logix
spencerh@ieee.org
+1 408 832 9616