EFLX®1K Logic/DSP eFPGA Target Spec

The EFLX1K is optimized for 40-180nm nodes where there is not a requirement for arrays of >20K LUTs and for small, fast control logic in applications like networking in 7-28nm nodes.

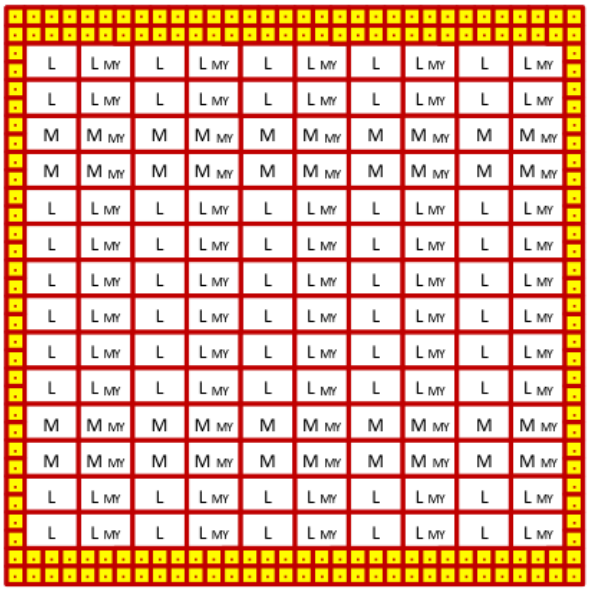
Both EFLX1K cores have 368 input pins, 368 output pins, XFLX™ interconnect network, multiple clocks & scan: fully reconfigurable in-field at any time.

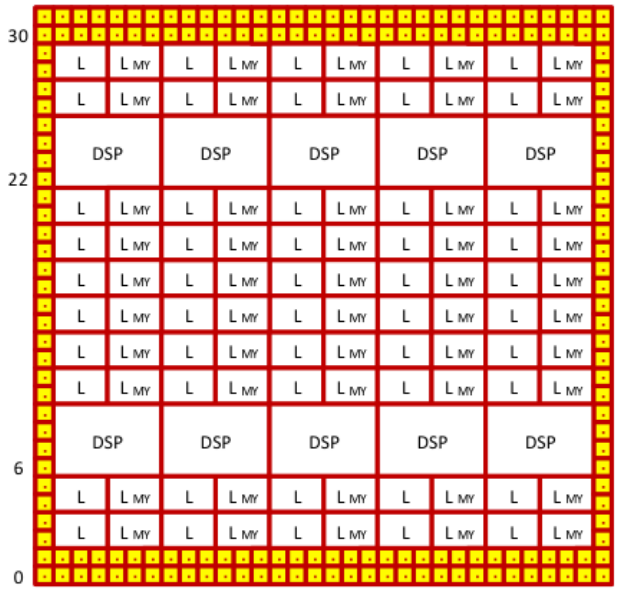
The EFLX1K Logic core has ~900 LUT4 and ~5Kbits distributed RAM; the DSP core has 10 of the 22x22 MACs (pre-adder, multiplier, accumulator) in two rows of 5 for pipelining between adjacent MACs for higher performance; the DSP core has ~650 LUT4.

Our Gen 2 XFLX™ programmable interconnect is optimized for high performance, high utilization and few metal layers for compatibility with most metal stacks.

This target spec is subject to change based on customer feedback.

Name	EFLX®1K eFPGA Core	
Technology	Any node in 6-8 months (after confirmed order and engineering resources available)	
Input and Output Pins	368 input & 368 output, each with an optional flip-flop	
Look-up Tables (6-input LUT with two independent outputs)	Logic Core	DSP Core
	560 LUT6 (~900 LUT4)	400 LUT6 (~650 LUT4)
Total Flip Flops (ex DSP)	1,836	1,536
Distributed Memory (Kb)	~5Kbits	-
DSP 22x22 MACs	-	10
EFLX Array Sizes Possible	1×1 to at least 7×7	





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